

Compal LA-K861P

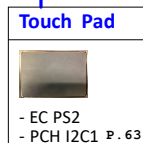
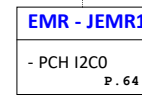
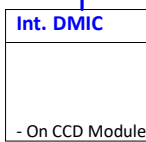
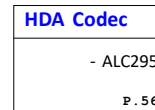
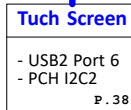
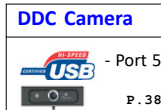
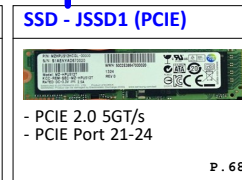
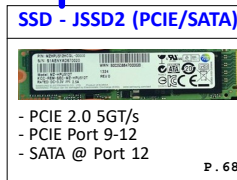
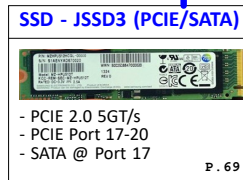
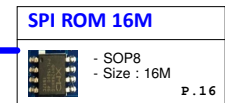
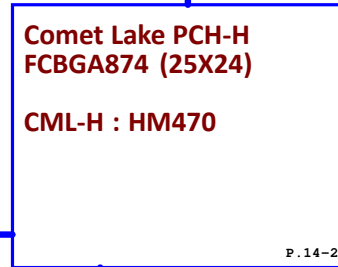
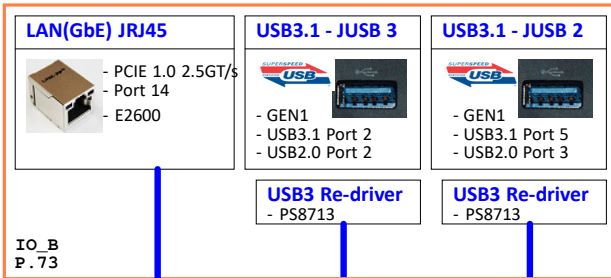
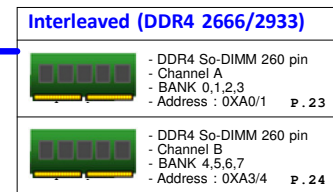
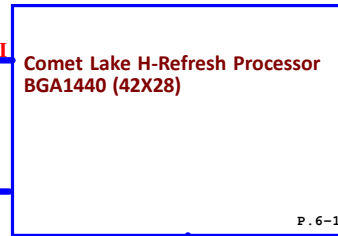
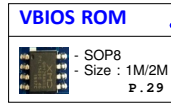
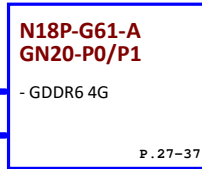
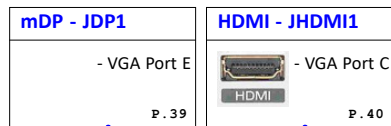
MB Schematic Document

GH51M

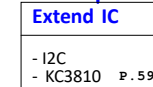
Rev:1.A

2020.11.19

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				Size Custom	Document Number
				GH51M M/B LA-K861P	
Date:				Tuesday, December 01, 2020	Sheet 1 of 112
					Rev 1A

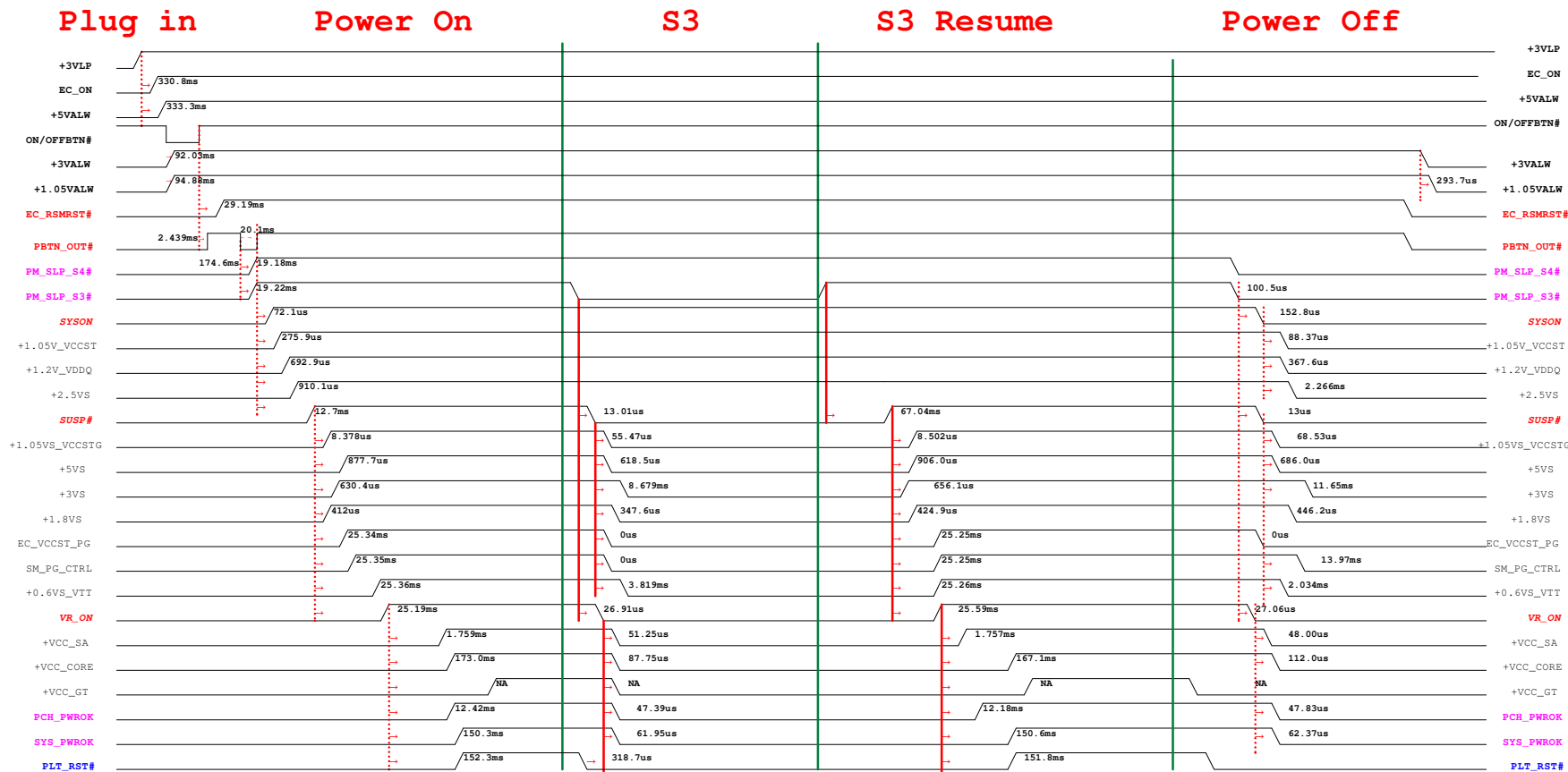


*Fan Control*2*
page 77



Sub Board	
IO/B (JIO1/JIO2)	P. 73
HS/B (JHS1)	P. 66
TURBO/B (JTRB1)	P. 77
RTC CKT. (JRTC1)	P. 20
Power On/Of f CKT	P. 63
HW Circuit DC/DC	P. 78
Power Circuit DC/DC	P. 82-111

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Date: Tuesday, December 01, 2020				Sheet 2	Rev 1A



Comet Lake-H Refresh

CPU

UC1 CMLRi52@
S IC CL8070104441108 SRK3X R1 2.4G ABO !
SA0000DW130

UC1 CMLRi53@
S IC CL8070104399510 SRH84 R1 2.5G ABO!
SA0000DCP40

UC1 CMLRi55@
S IC CL8070104409309 SRK3Z R1 2.5G ABO !
SA0000E0Y20

UC1 CMLRi77@
S IC CL8070104399315 SRH8Q R1 2.6G ABO !
SA0000DCN40

UC1 CMLRi78@
S IC CL8070104399317 SRK3Y R1 2.2G ABO!
SA0000DW230

PCH

UH1 CMLPCH@
S IC FH82HM470 SRJAU A0 FCBGA PCH-H ABO!
SA0000DDP80

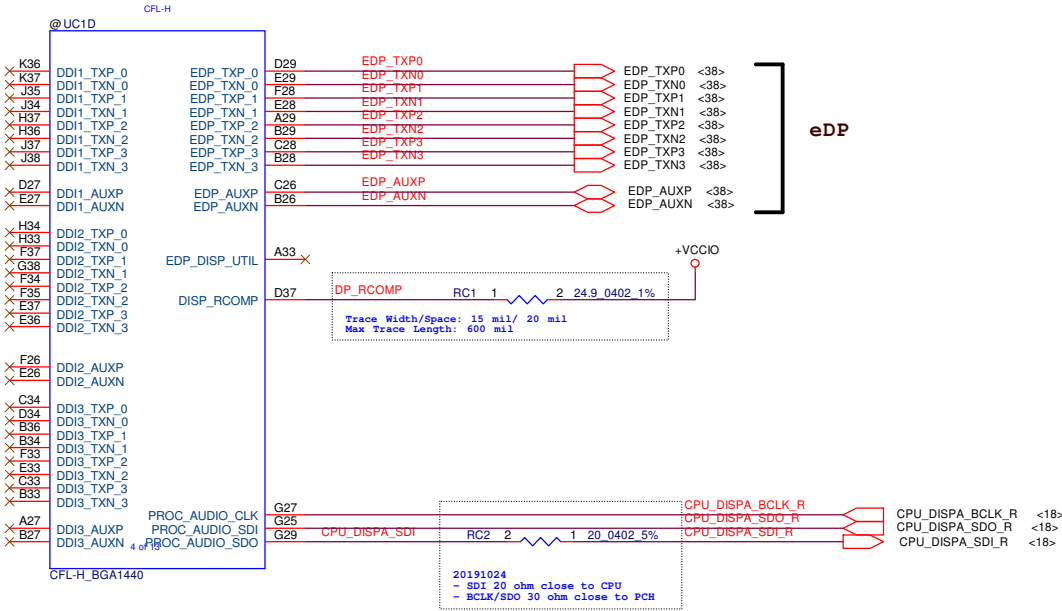
NVIDIA

UV1 N18PA@
S IC N18P-G61-A-A1 BGA 1358 GPU ABO !
SA0000DVM50

UV1 N20Z@
S IC N20Z-QS1-A1 QS1 BGA 1358 S
SA0000E1W10

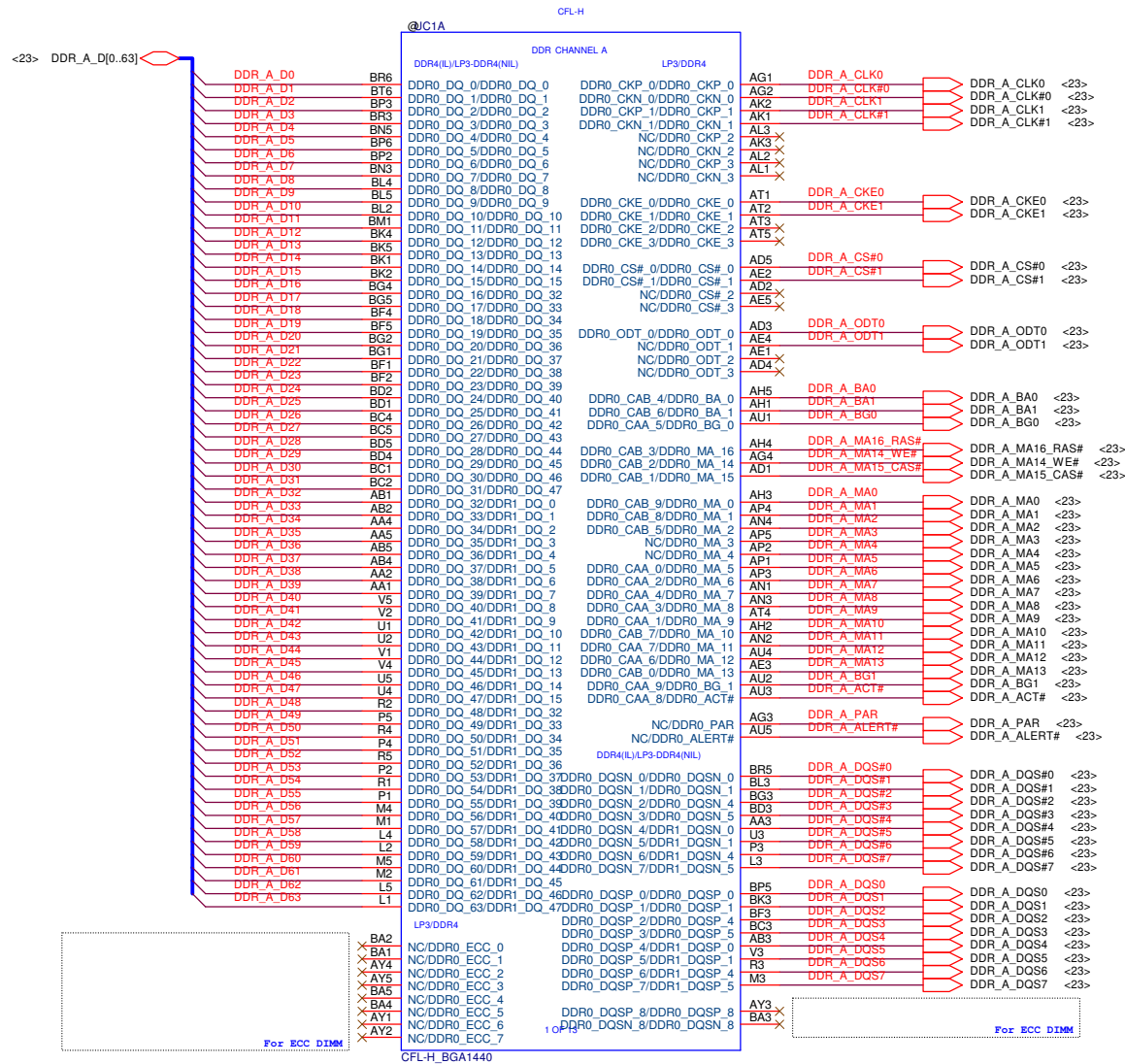
PCB

ZZZ PCB@
PCB 3AU LA-K861P REV0 MB 4 S
DAA0000Q000



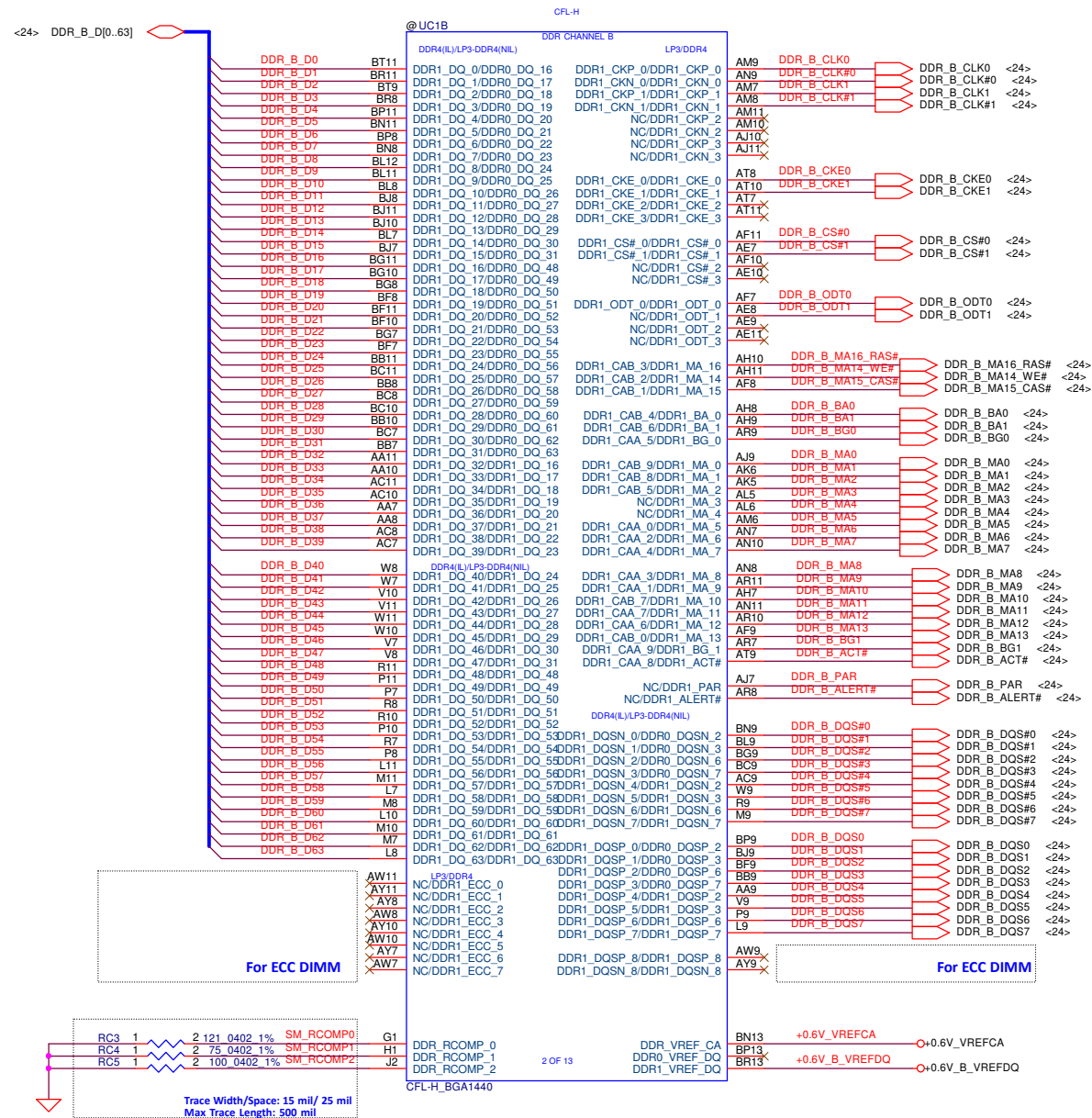
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								Custom	GH51M M/B LA-K861P		1A
								Date: Tuesday, December 01, 2020			

CHANNEL-A Interleaved Memory



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						Size	Document Number		Rev			
						Custom	GH51M M/B LA-K861P		1A			
						Date:	Tuesday, December 01, 2020		Sheet	7	of	112

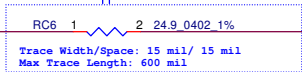
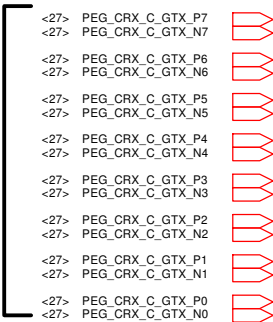
CHANNEL-B Interleaved Memory



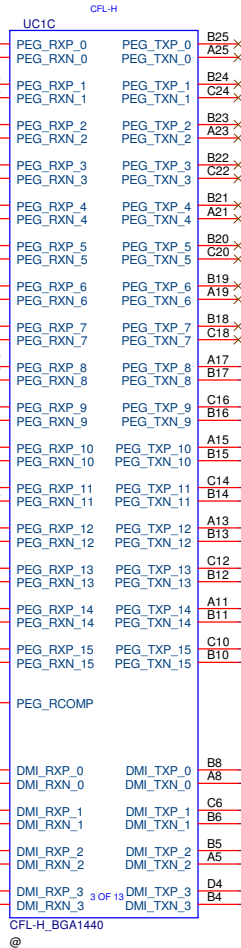
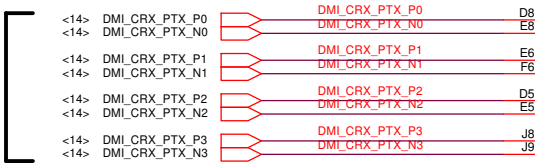
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				Customer	GH51M M/B LA-K861P Rev 1A
				Date:	Tuesday, December 01, 2020 Sheet 8 of 112

PEG&DMI

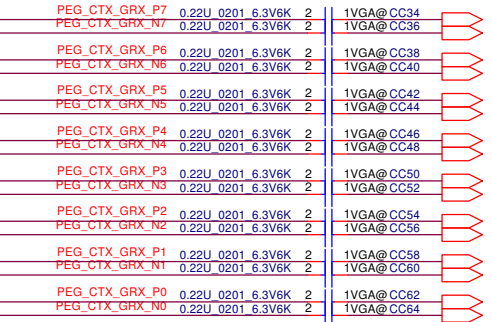
To N18PG61A / N20P DGPU x 8 Lane



To PCH



To N18PG61A / N20P DGPU x 8 Lane



To PCH

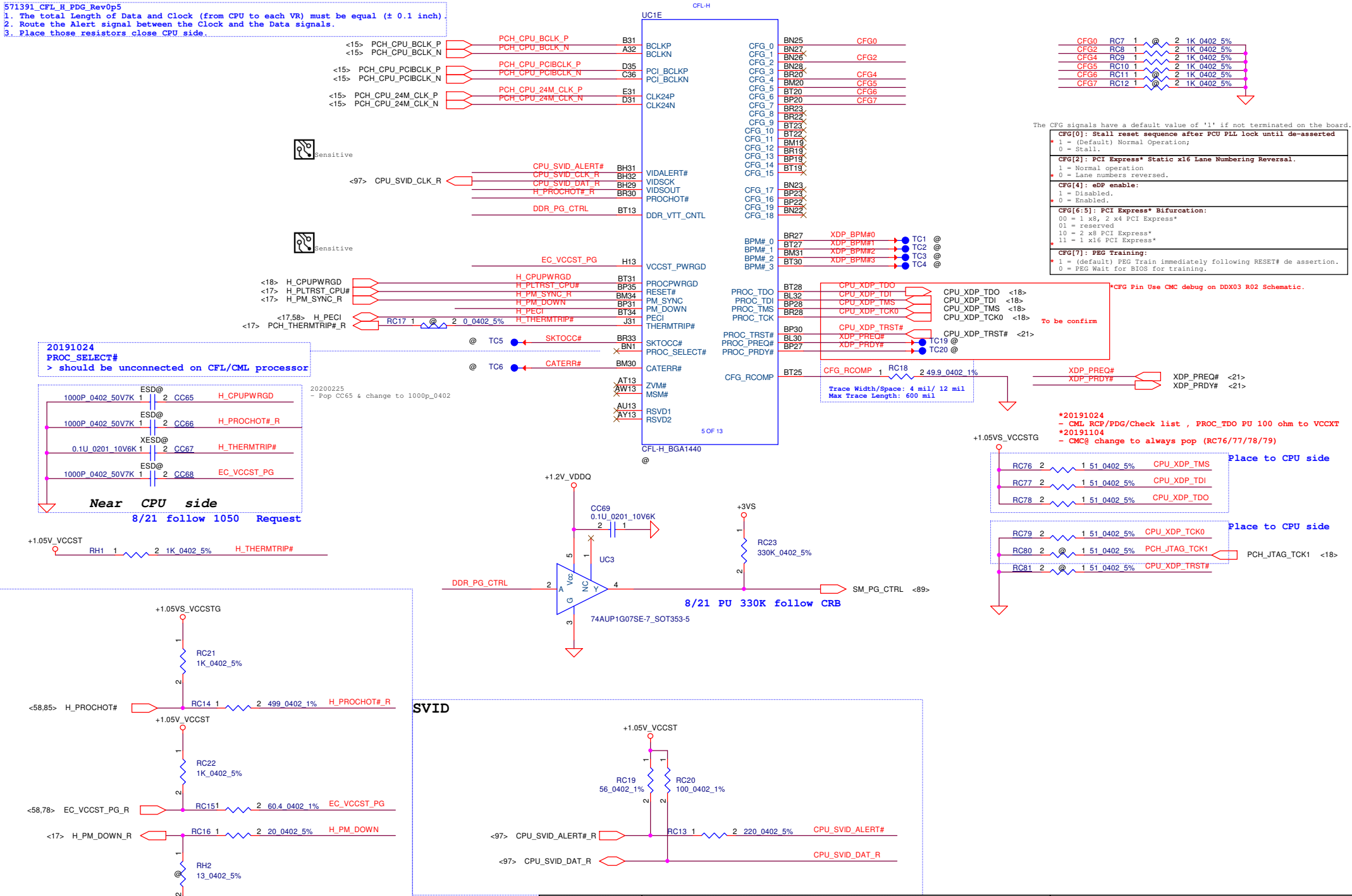


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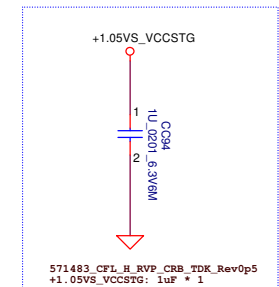
1. The total Length of Data and Clock (from CPU to each VR) must be equal (± 0.1 inch)

2. Route the Alert signal between the Clock and the Data signals.

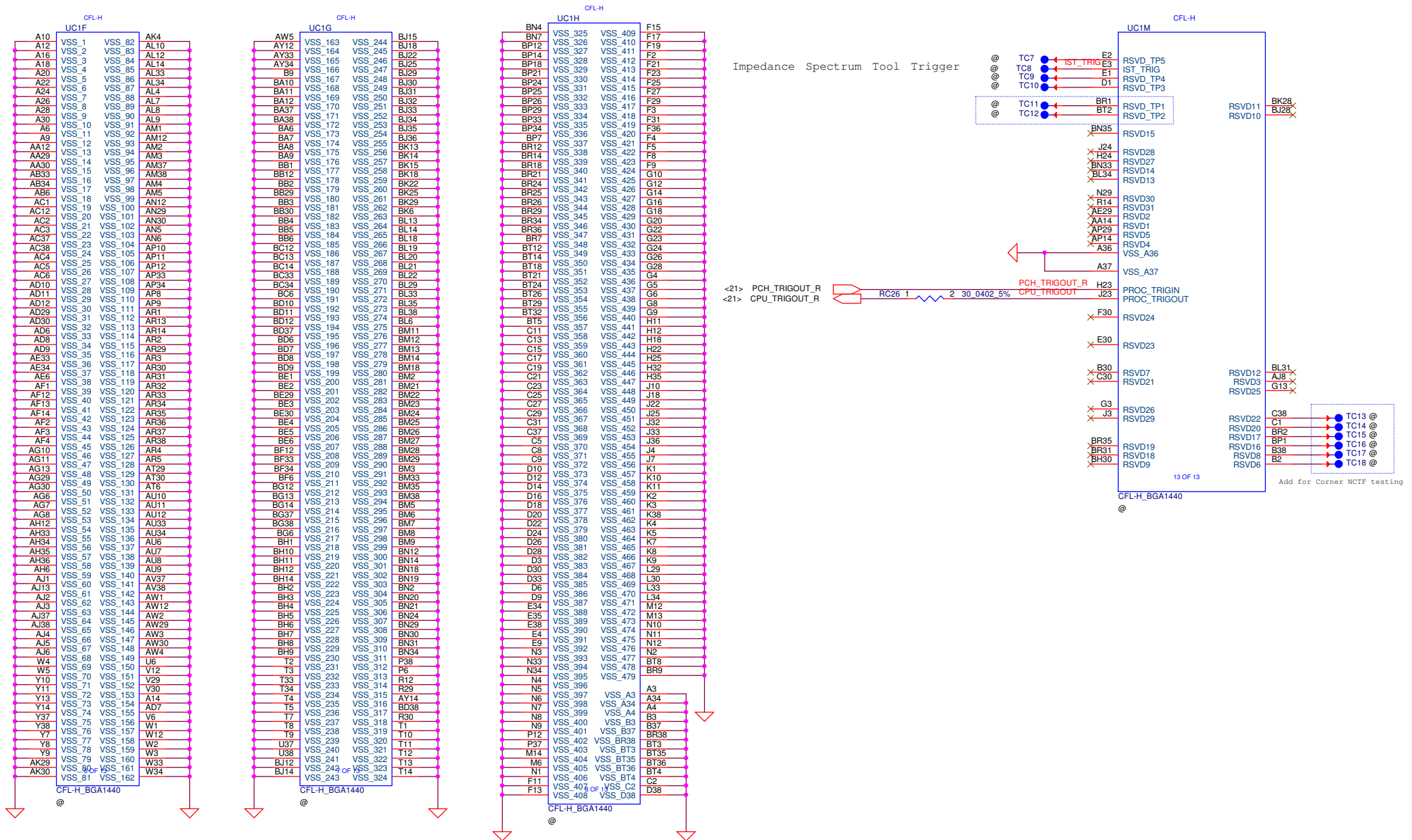
3. Place those resistors close CPU side.

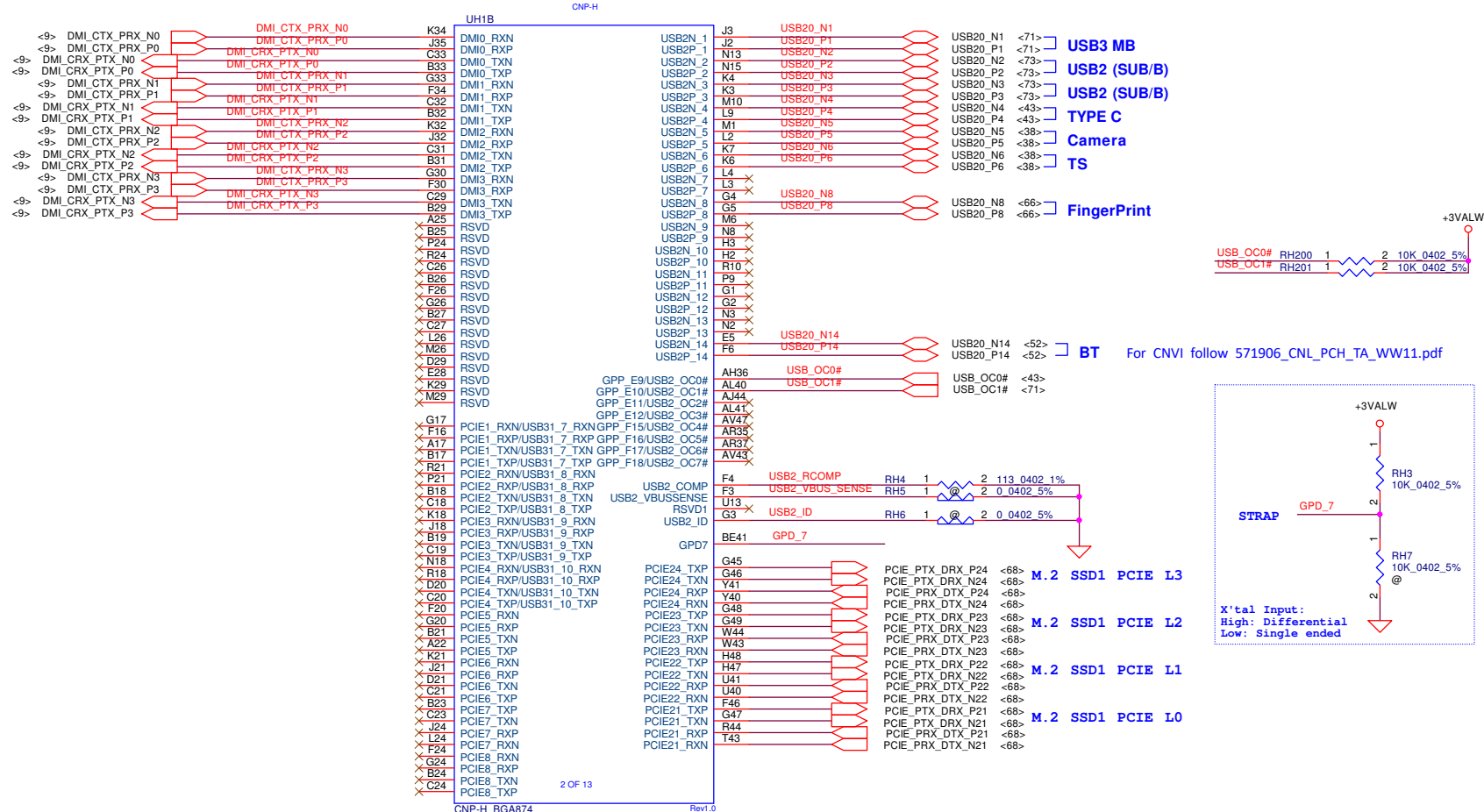






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				CFL-H(7/8)VCCSA/VCCIO/VDDQ					
				Size	Document Number		Rev		
				Custom	GH51M M/B LA-K861P		1A		
Date:				Tuesday, December 01, 2020		Sheet	12	of	112

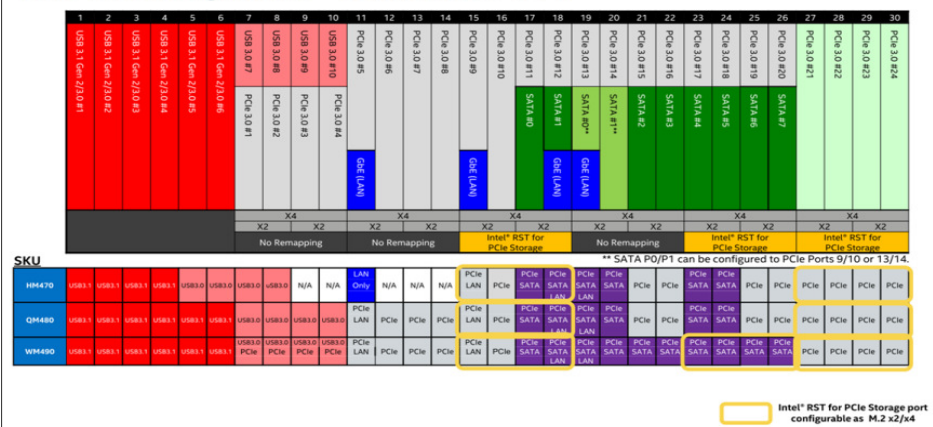


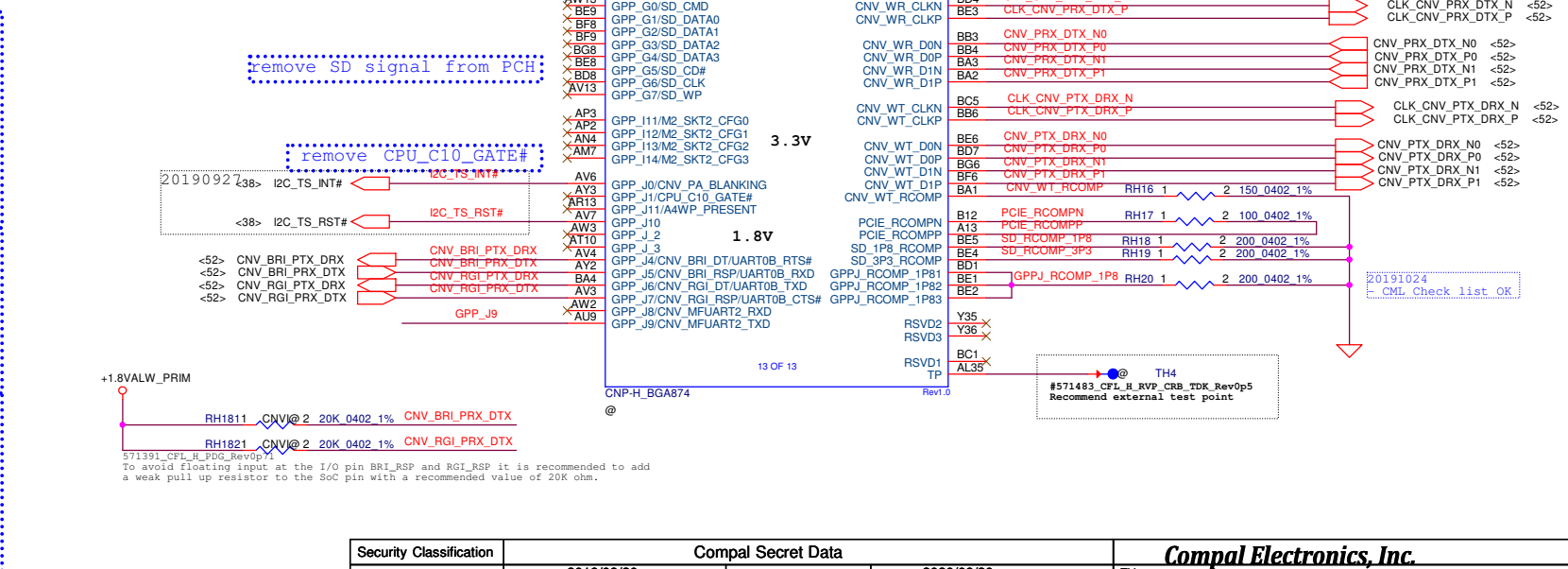
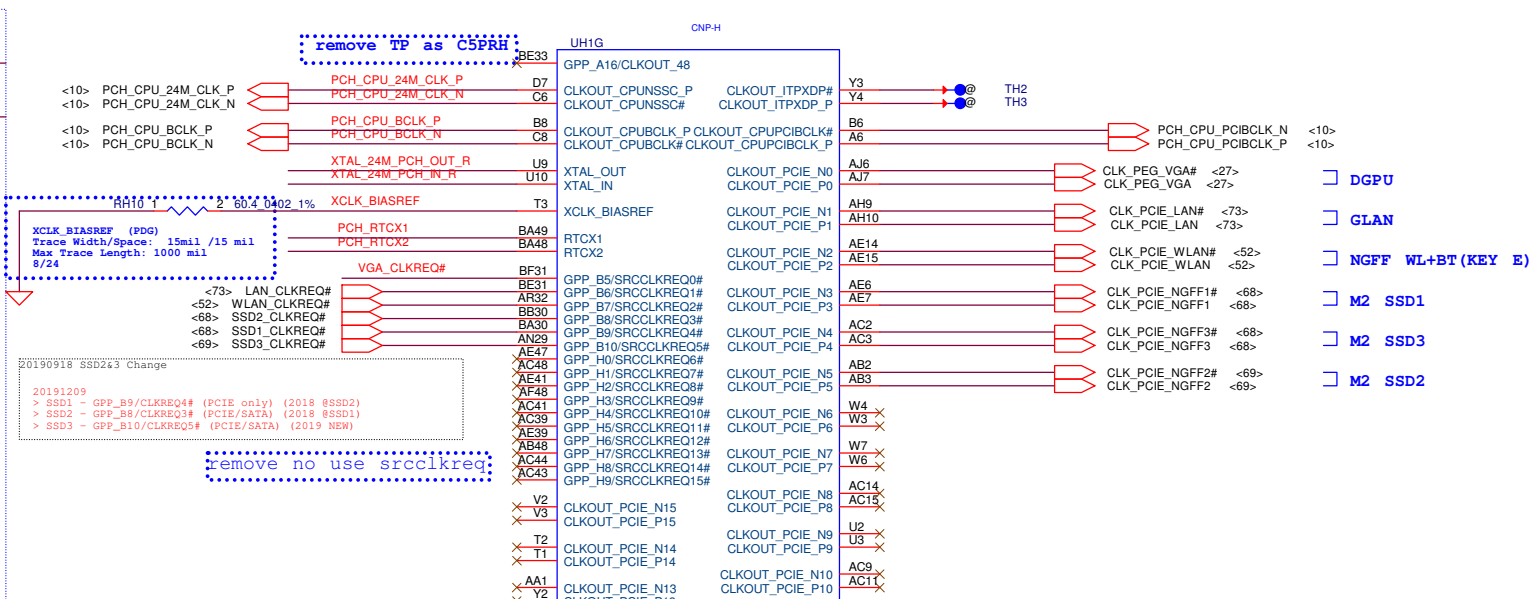


The 30 HSI0 lanes on PCH-H supports the following configurations:

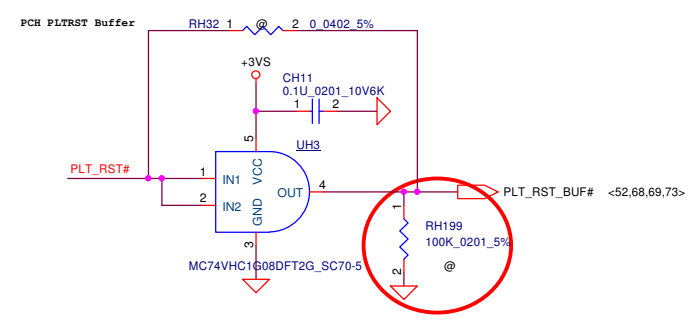
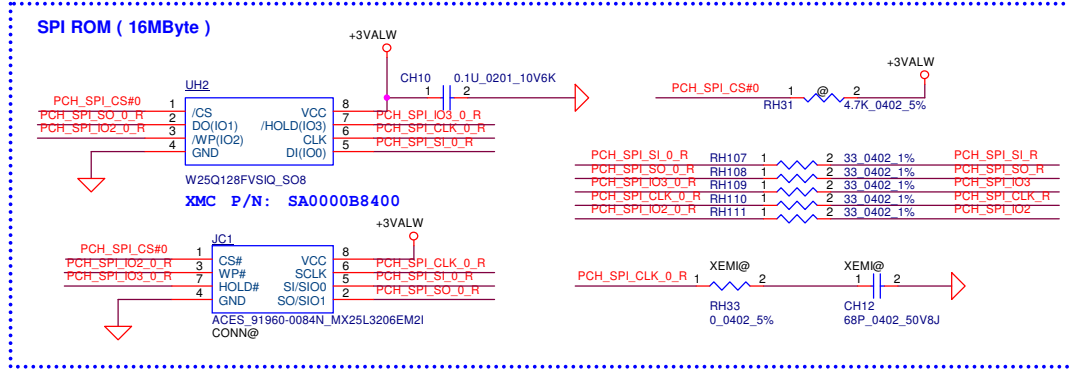
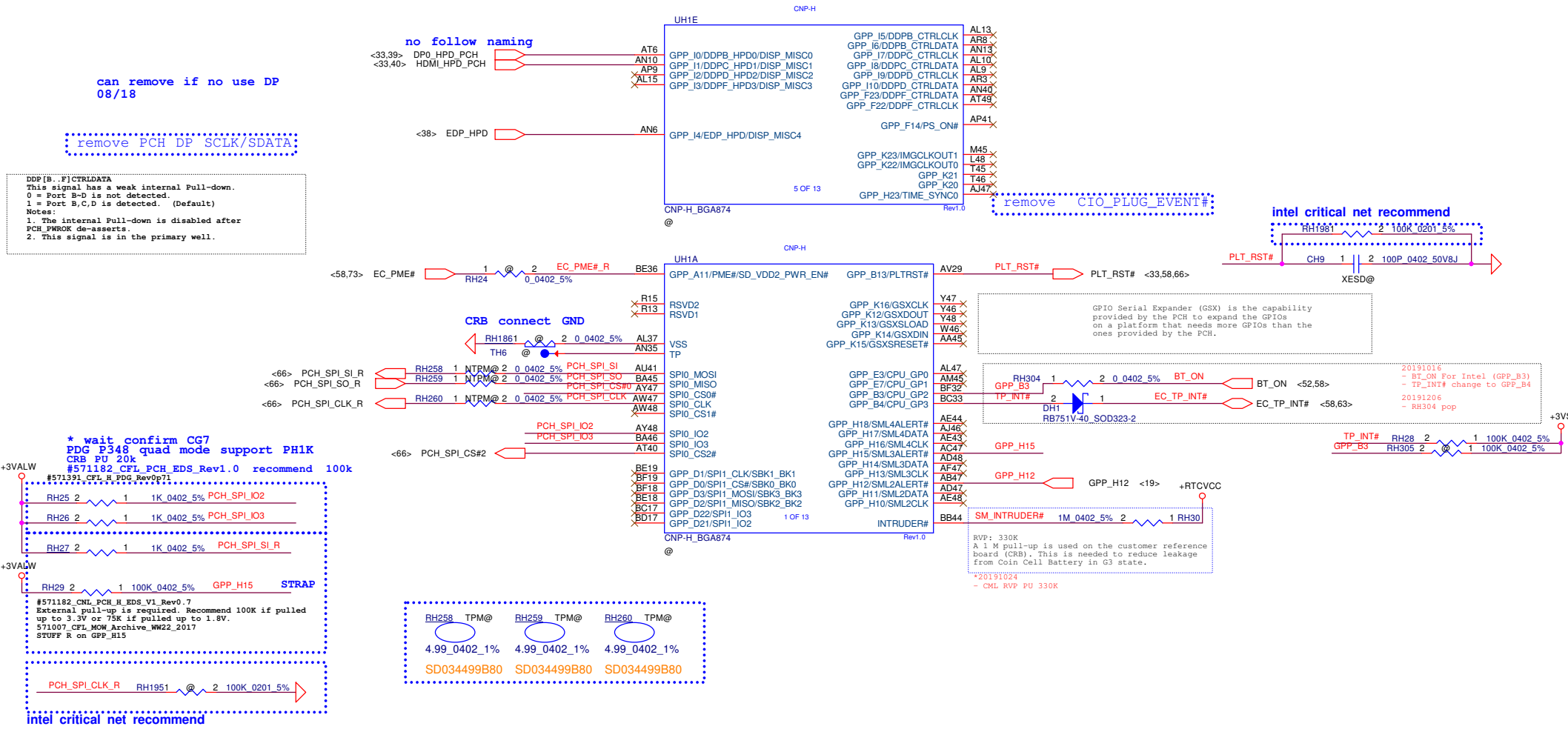
- Up to 24 PCIe* Lanes
 - A maximum of 16 PCIe* Ports (or devices) can be enabled
 - When a GBE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
 - PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
- Up to 6 SATA Lanes
 - A maximum of 6 SATA Ports (or devices) can be enabled
 - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
 - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
 - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 4 GbE Lanes
 - A maximum of 1 GbE Port (or device) can be enabled
- Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
 - x2 and x4 PCIe* NVMe SSD
 - x2 IntelR Optane? Memory Device
 - See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers, configuration, and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support
- For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe* Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

HSIO Lane Assignments – Comet Lake PCH-H

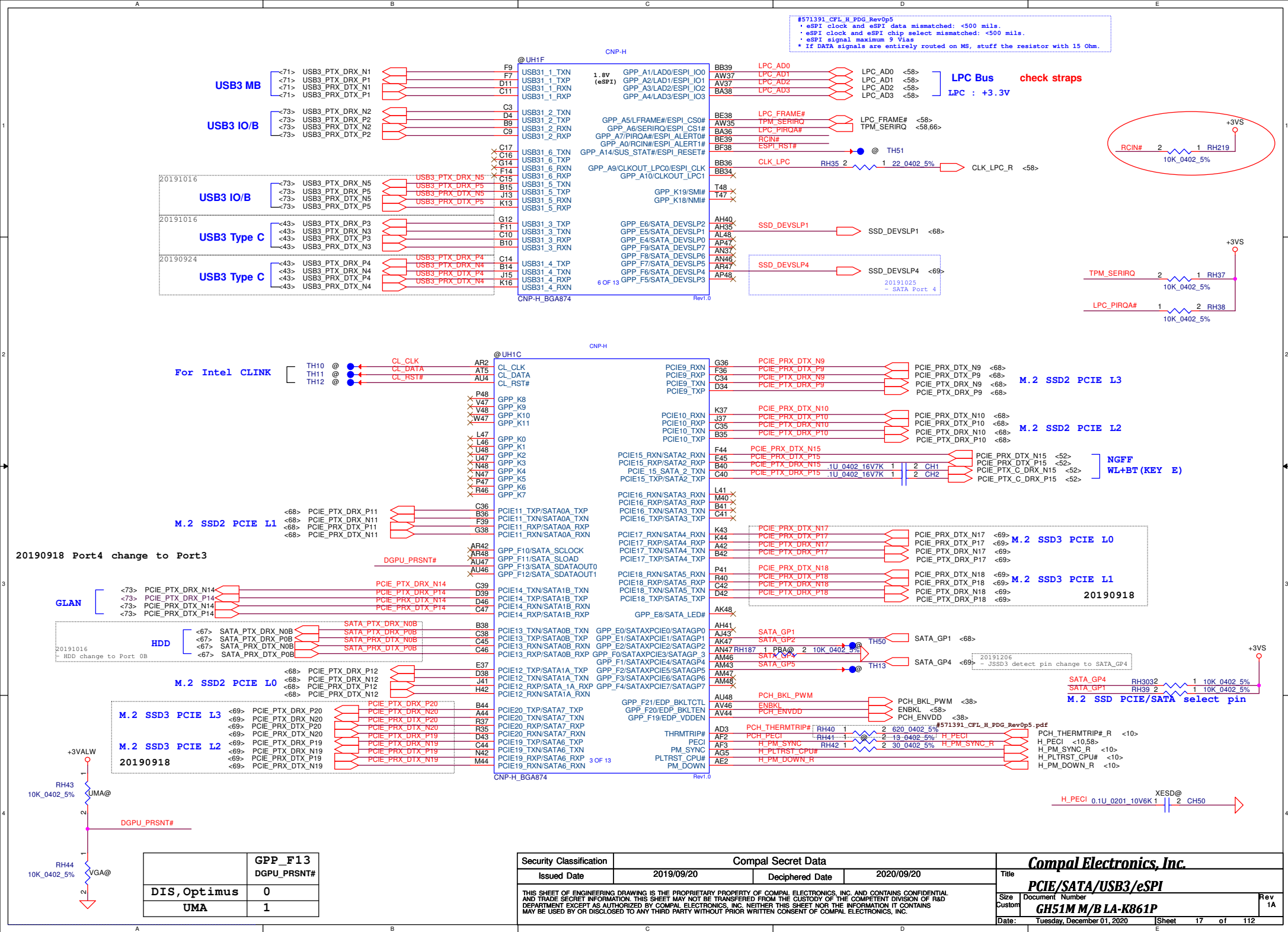


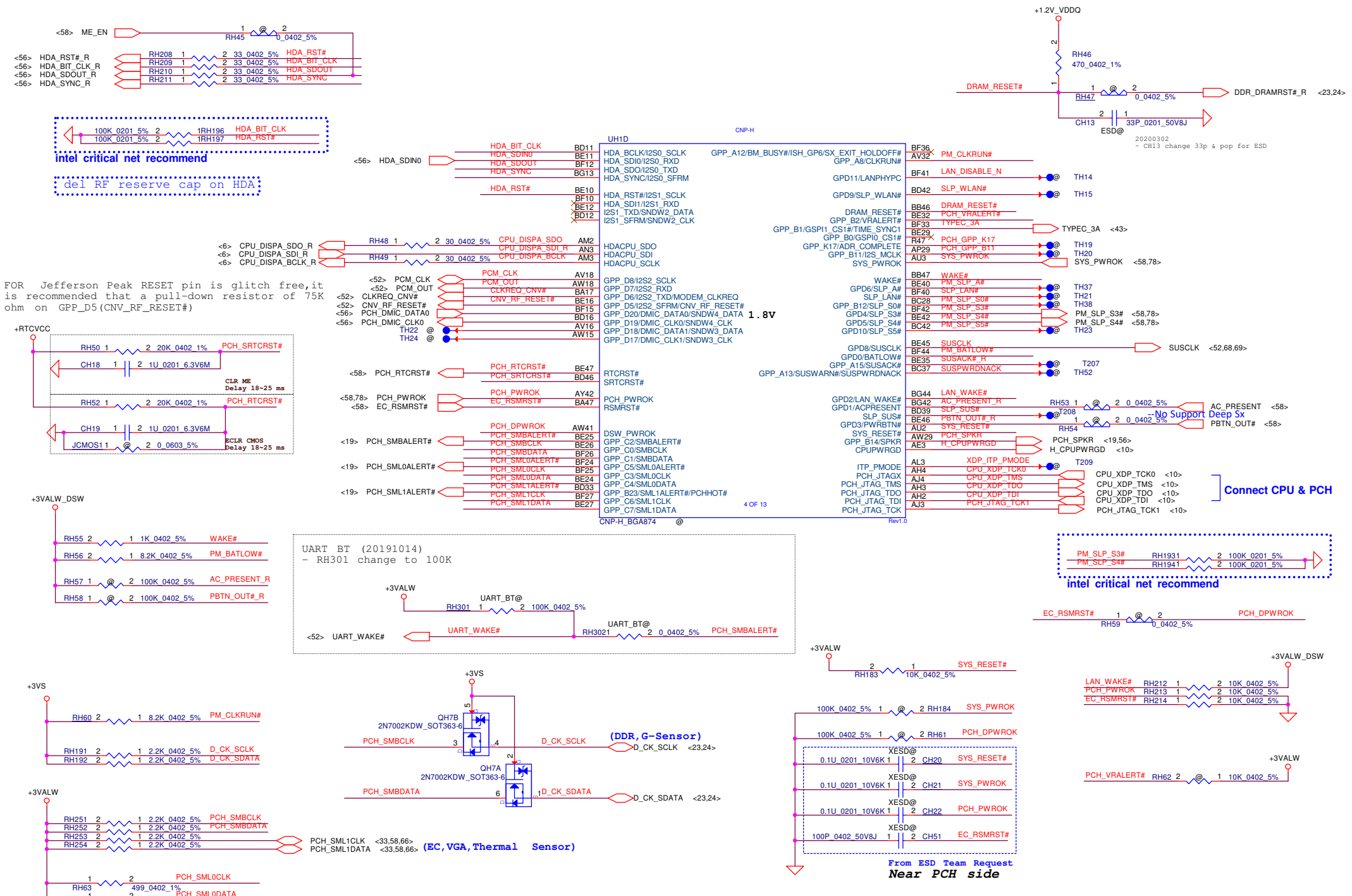


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				Customer	GH51M M/B LA-K861P Rev 1A
				Date:	Tuesday, December 01, 2020 Sheet 15 of 112



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						PCH(3/8)DDC/SPI			
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				Custom	GH51M M/B LA-K861P	1A			
				Date:	Tuesday, December 01, 2020	Sheet	16	of	112



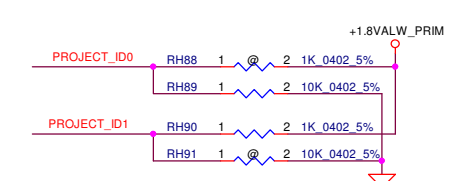
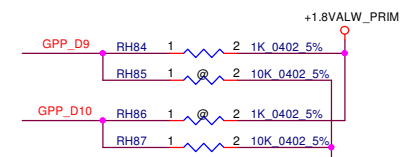
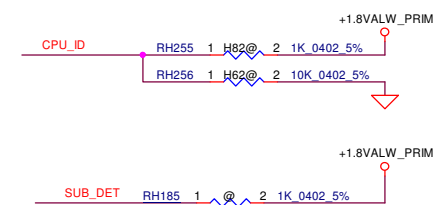


FOR Jefferson Peak RESET pin is glitch free,it is recommended that a pull-down resistor of 75K ohm on GPP_D5(CNV_RF_RESET#)

--No Support Deep Sx
PBTN_OUT# <58>

Connect CPU & PCH

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Size		Document Number				Rev 1A
Custom		GH51M M/B LA-K861P				
Date:		Tuesday, December 01, 2020		Sheet 18 of 112		



Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
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NA	0	1
*Gaming 50	1	0
Gaming 60	1	1

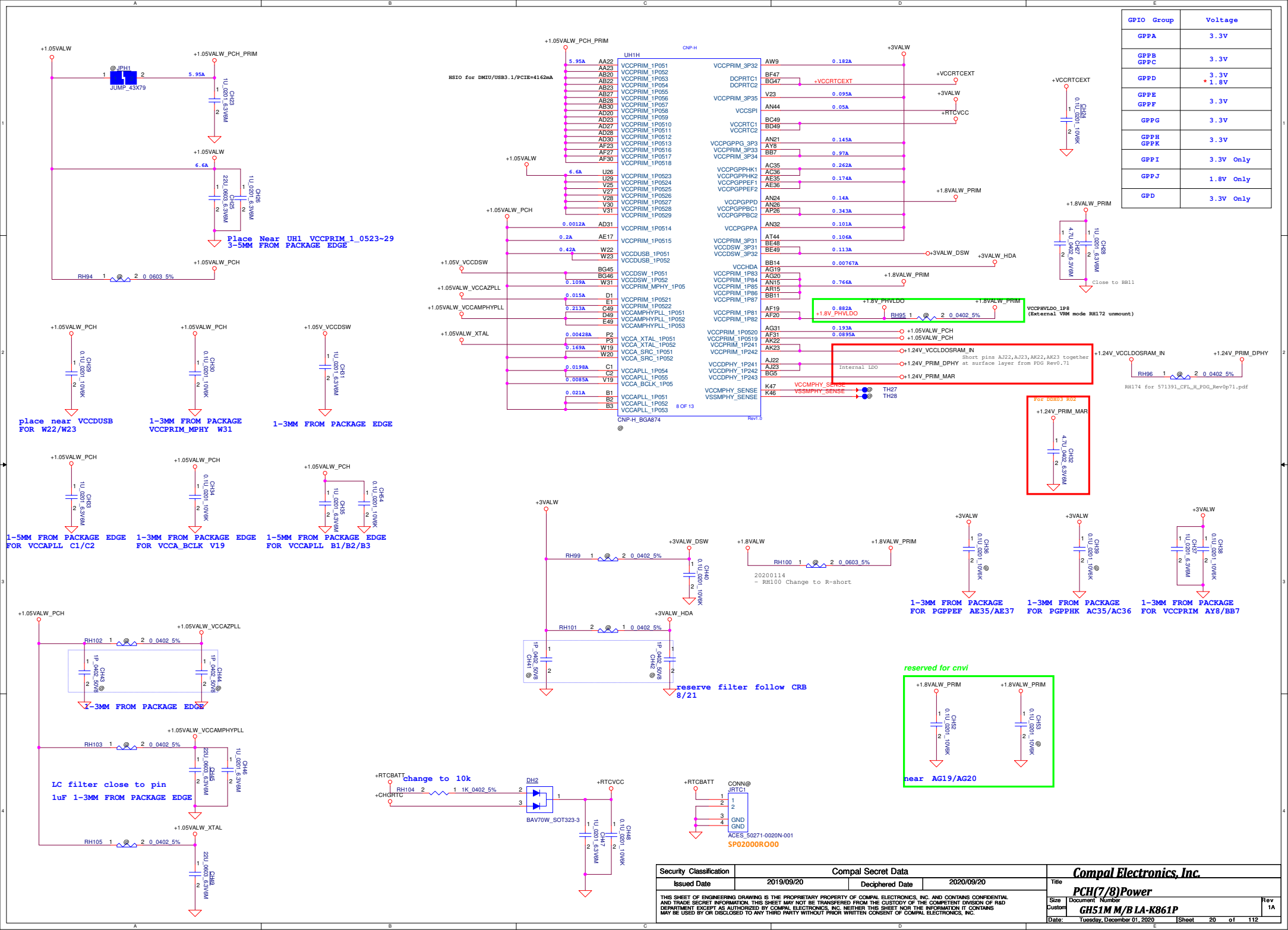
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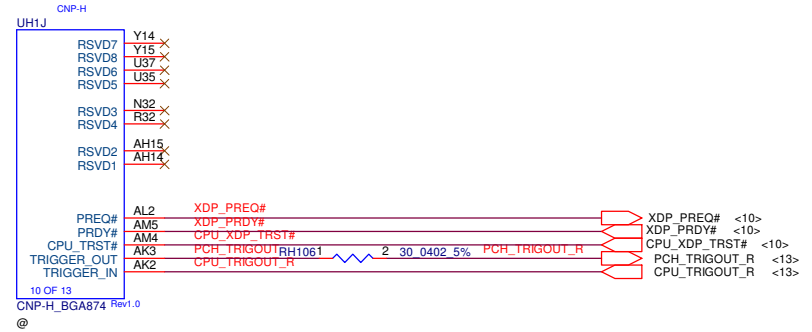
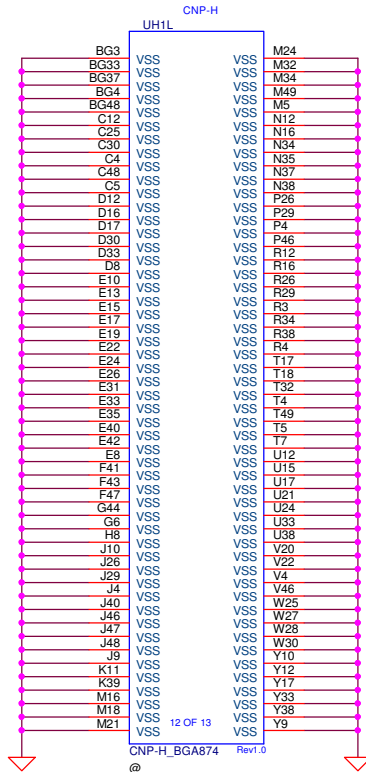
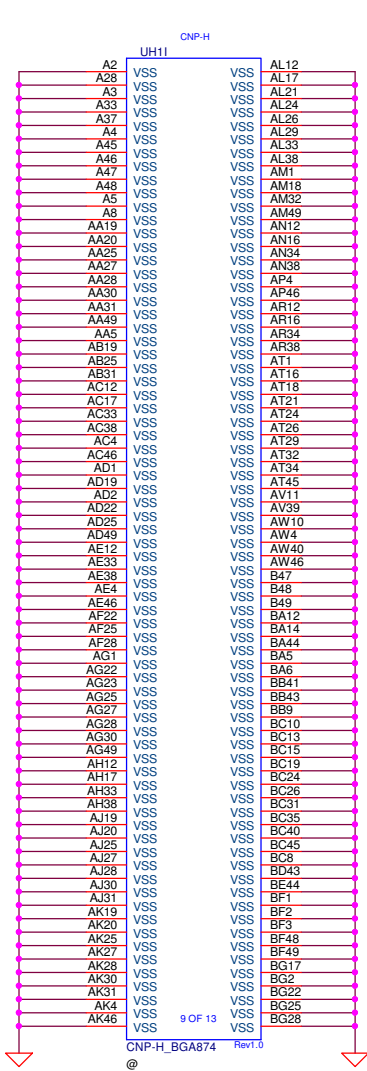
SCI capability is available on all GPIOs
PCH GPIOs that can be routed to generate SMI# or NMI:
  * GPP_B[4], GPP_B[20], GPP_B[23]
    * GPP_C[23:22]
    * GPP_D[4:0]
    * GPP_E[8:0]
    * GPP_I[3:0]
  * GPP_G[7:0] (support SMI# only).

The voltage of all GPIO pads in each GPP group is determined by the voltage supplied to the group (either 3.3V or 1.8V),
except for GPP_I and GPP_D group, (which are 3.3V only), and GPP_J group (which is 1.8V only).

All GPIOs have programmable internal pull-up/pull-down resistors which are off by default.
The internal pull-up/pull-down for each GPIO can be enabled by BIOS programming.

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						Size		Document Number		Rev	
						Custom		GH51M M/B LA-K861P		1A	
Date:		Tuesday, December 01, 2020		Sheet		21		of 112			

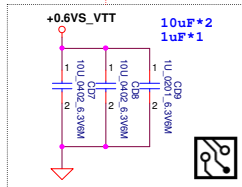
Reserve Page

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				Date: Tuesday, December 01, 2020	GH51M M/B LA-K861P	1A
				Sheet	22	of 112

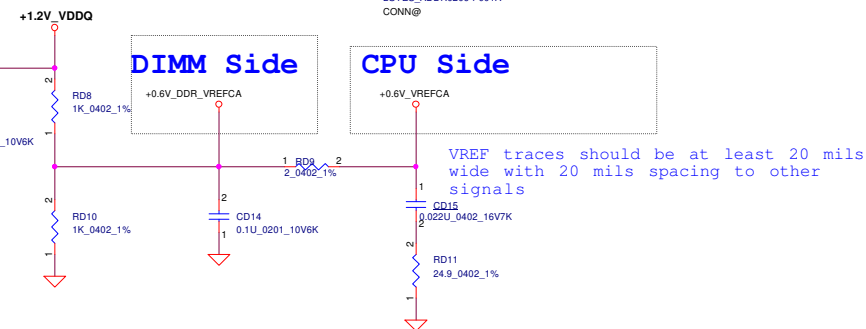
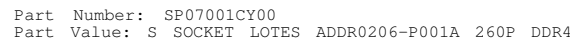
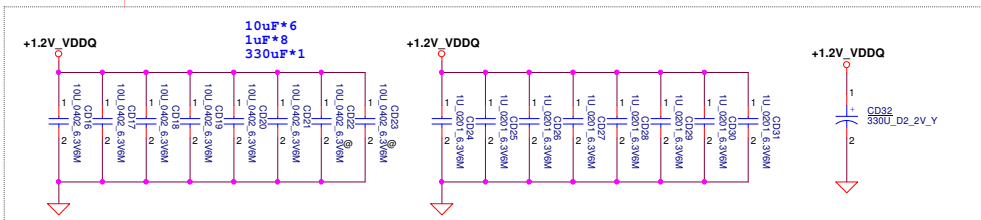
> Non-ECC SO-DIMM

STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM1.258



Layout Note:
Place near JDIMM1



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				GH51M M/B LA-K861P		
				Date:	Tuesday, December 01, 2020	Sheet 23 of 112

CHANNEL-B (Interleaved Memory)

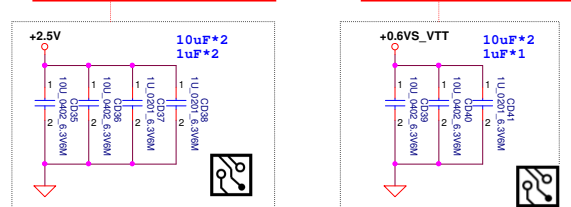
> BOT : STD type (4mm)

> Non-ECC SO-DIMM

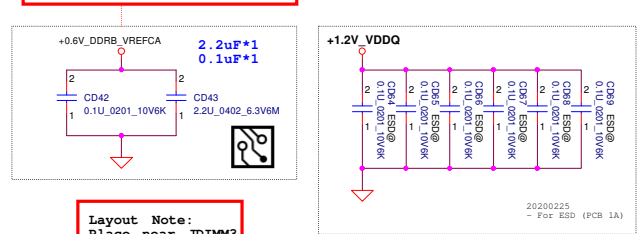
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

Layout Note:
Place near JDIMM3.257,259

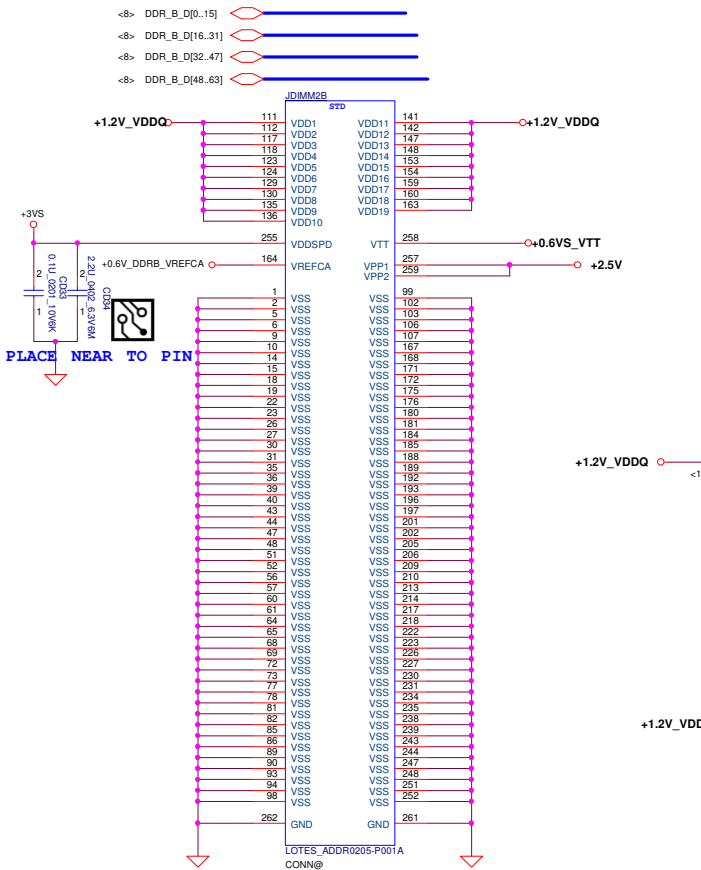
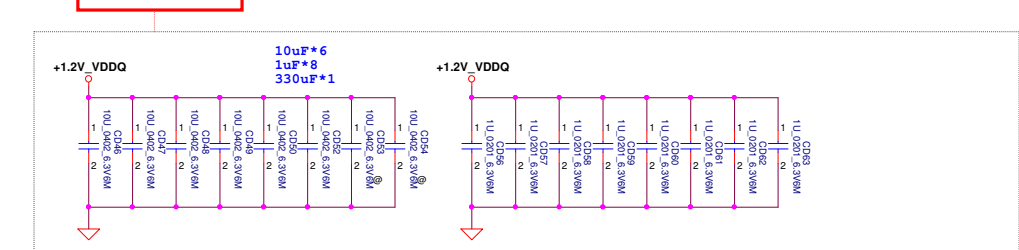
Layout Note:
Place near JDIMM3.258



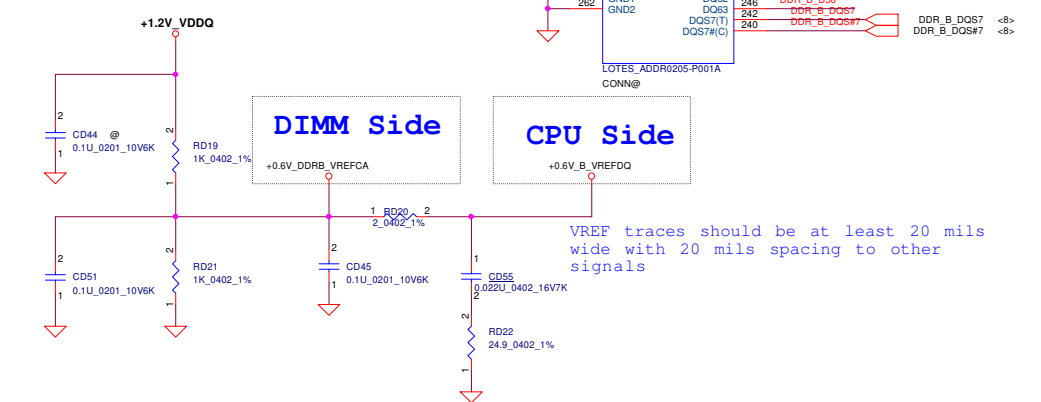
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



Layout Note:
Place near JDIMM3



Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD



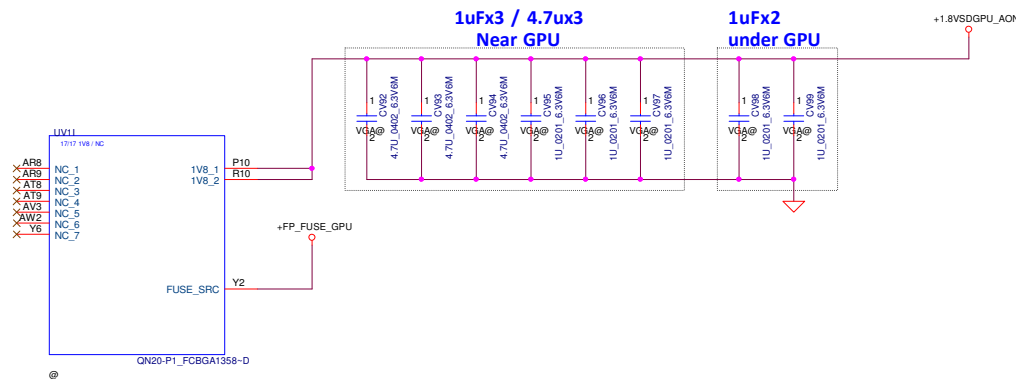
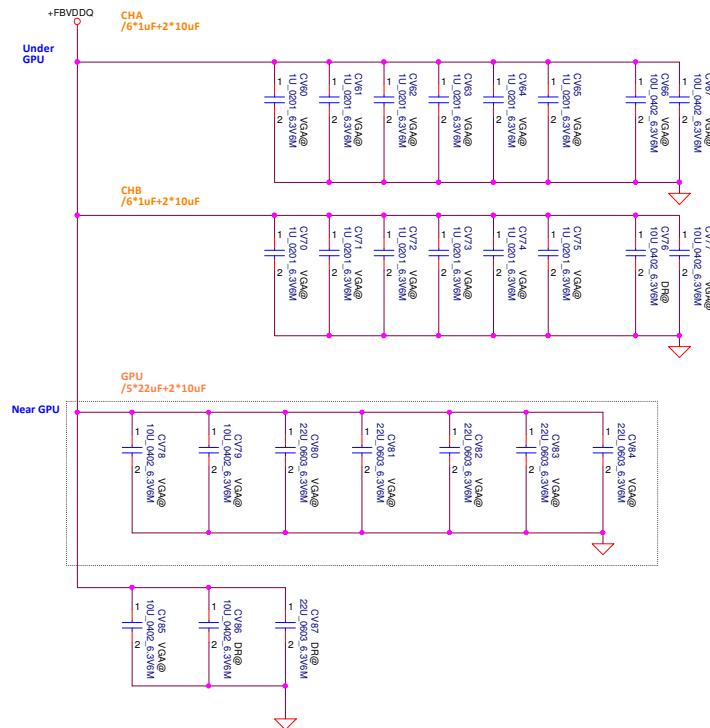
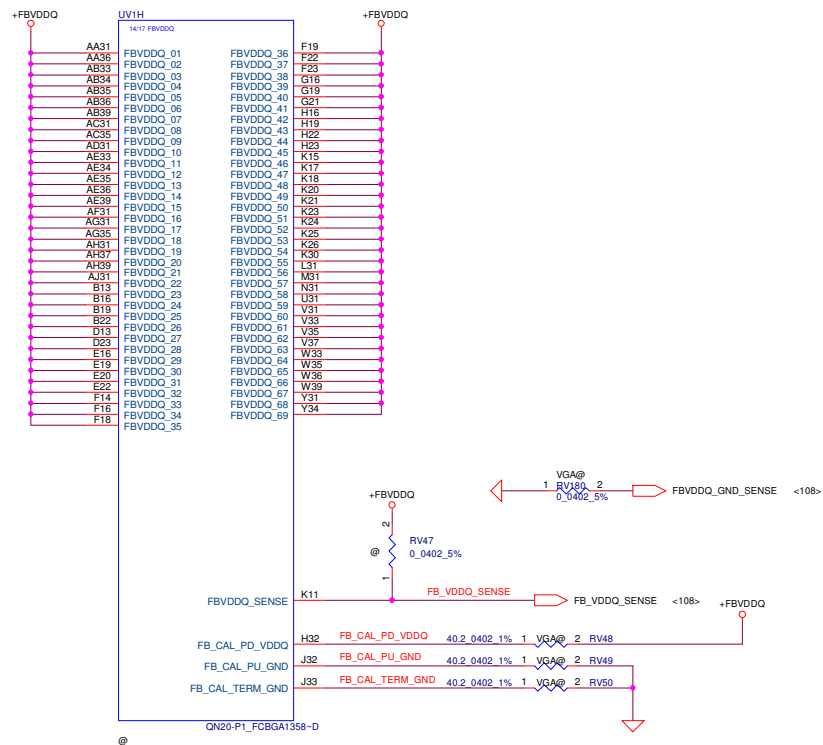
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
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						Size Document Number		1A			
						GH51M M/B LA-K861P					
						Date		Tuesday, December 01, 2020		24 of 112	

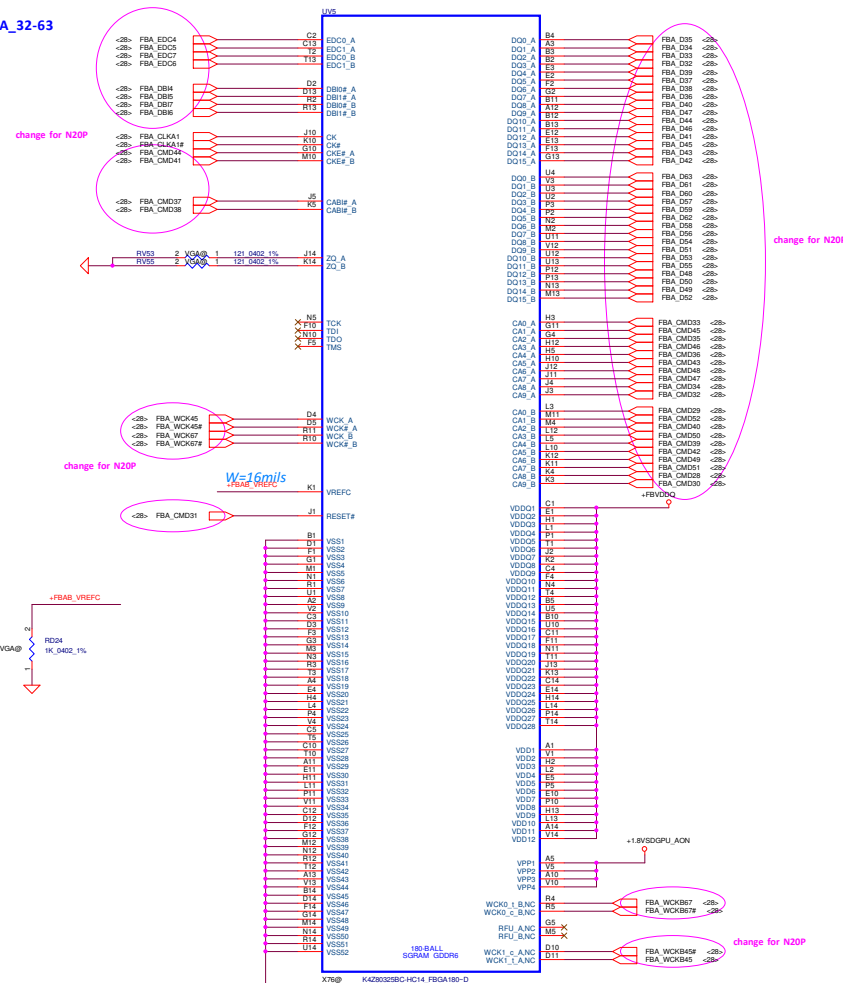
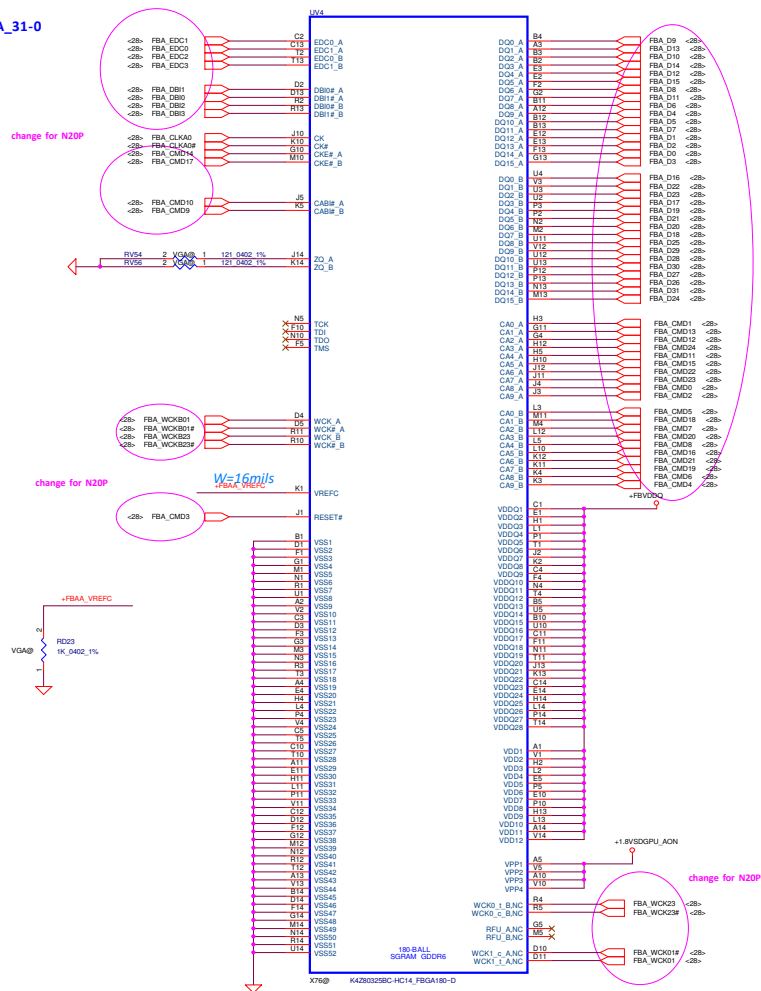
Reserve Page

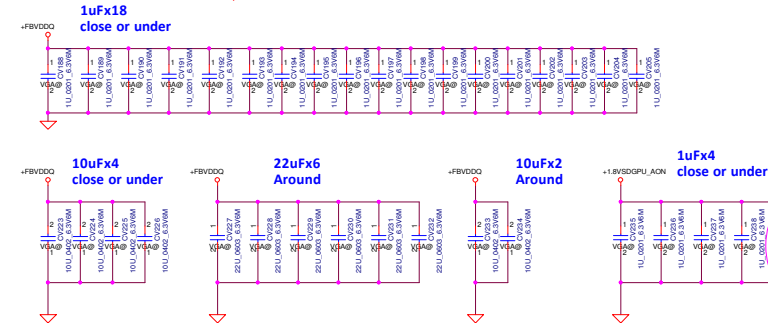
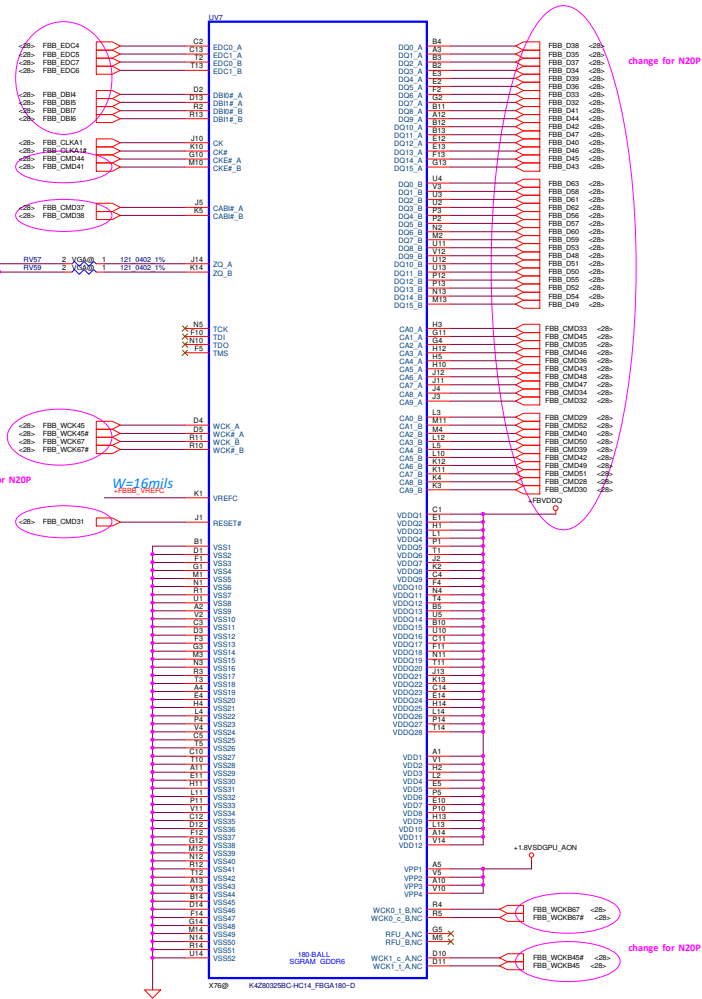
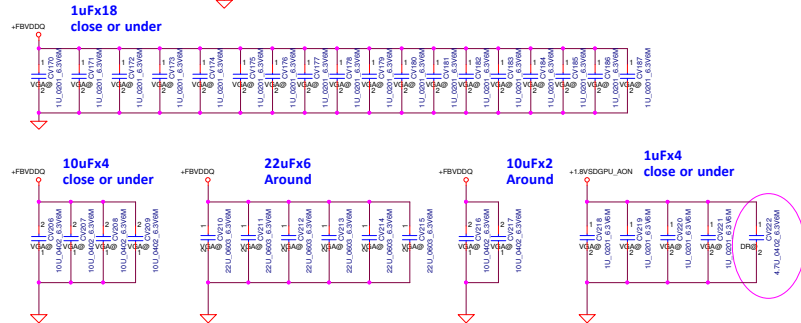
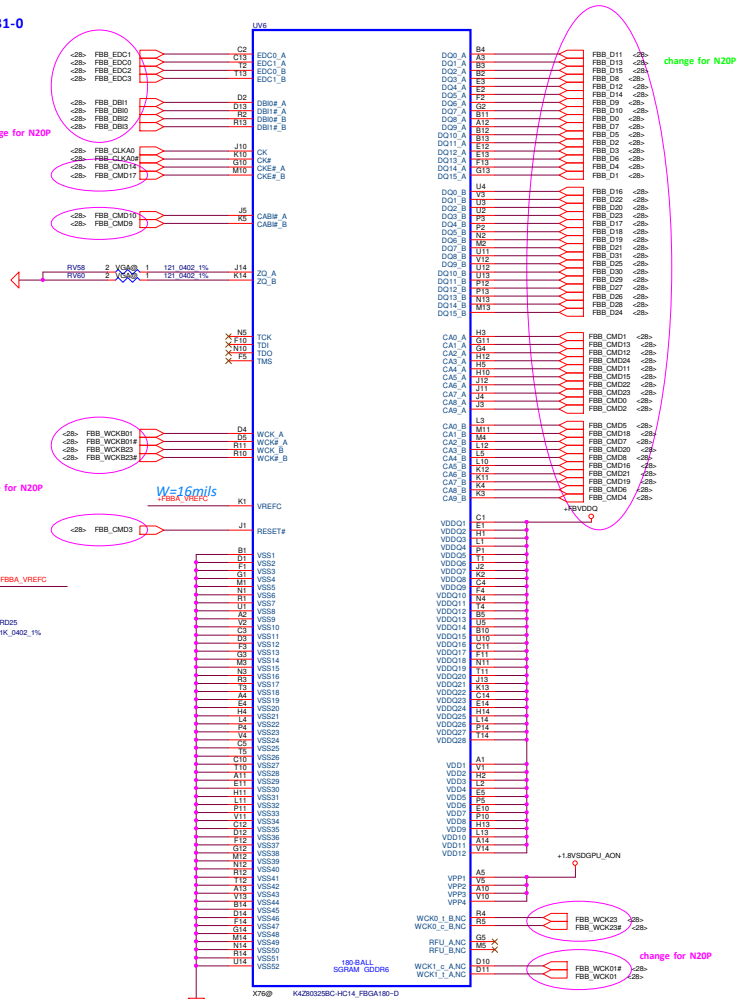
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					GH51M M/B LA-K861P	1A
				Date:	Tuesday, December 01, 2020	Sheet 25 of 112

Reserve Page

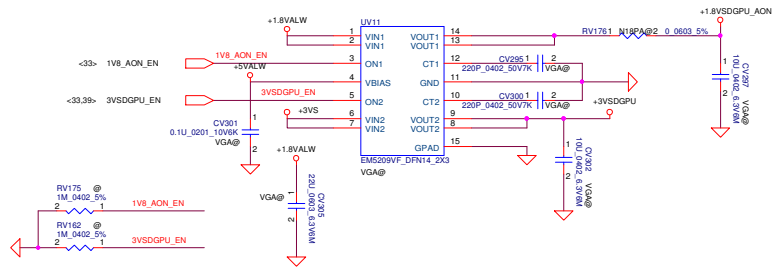
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Issued Date	2019/09/20	Deciphered Date	2020/09/20	Title	Reserve	
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					GH51M M/B LA-K861P	1A
				Date:	Tuesday, December 01, 2020	Sheet 26 of 112



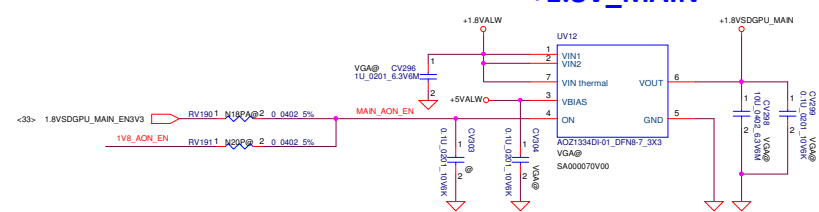




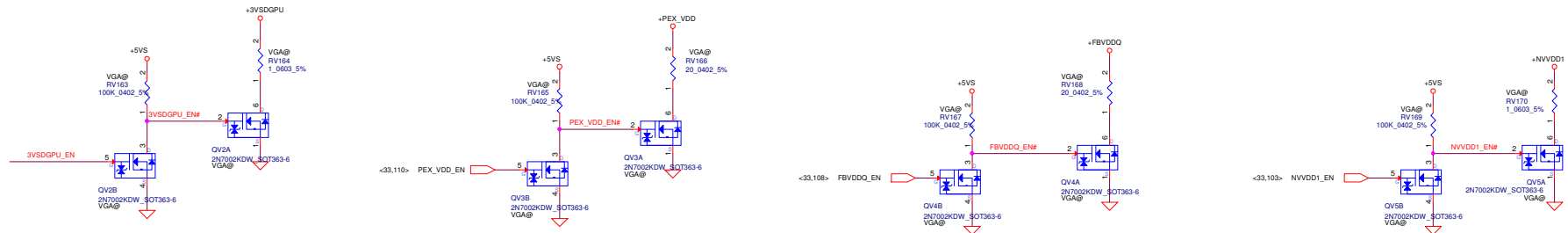
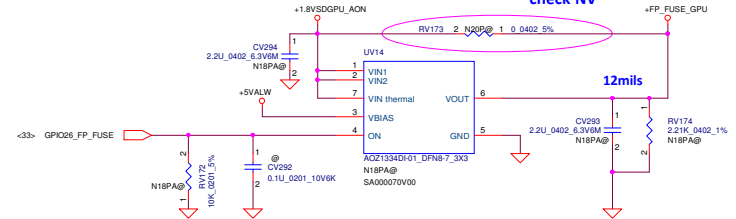
+1.8V_AON/+3VSDGPU



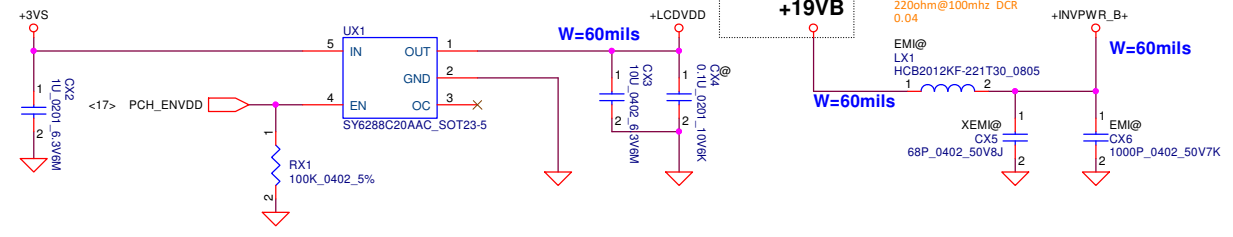
+1.8V_MAIN



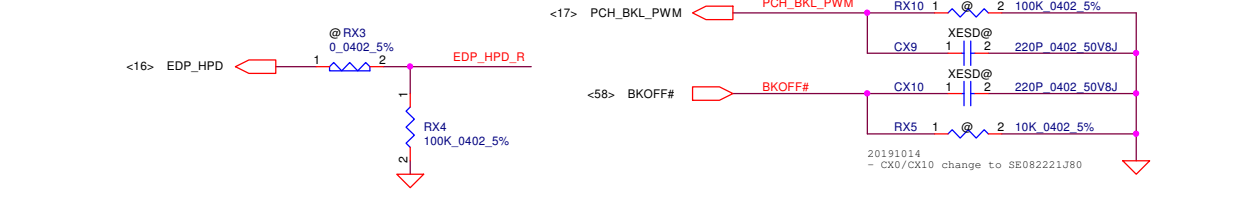
check NV



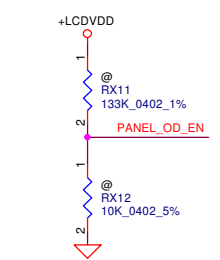
LCD POWER CIRCUIT



LCD enable signal

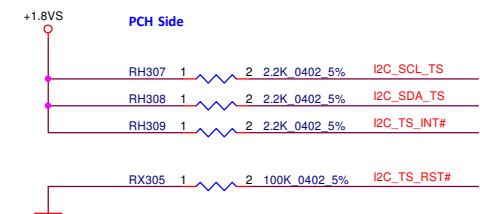
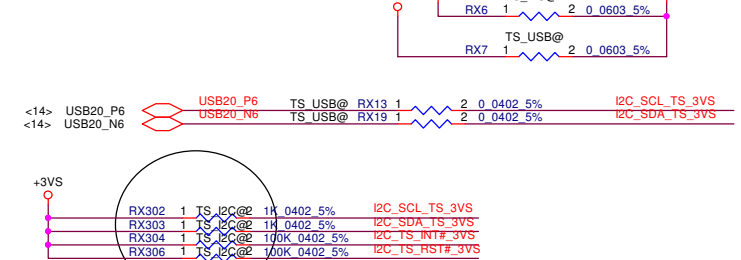


Panel OD

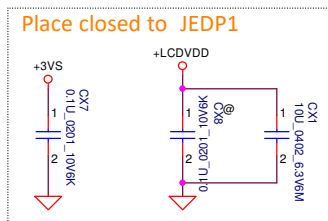
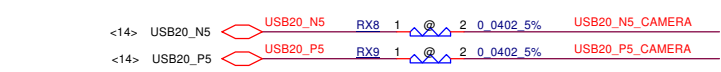


20190506
- RX11 change to unpop
- B103 needs to detect panel
to select H or L.

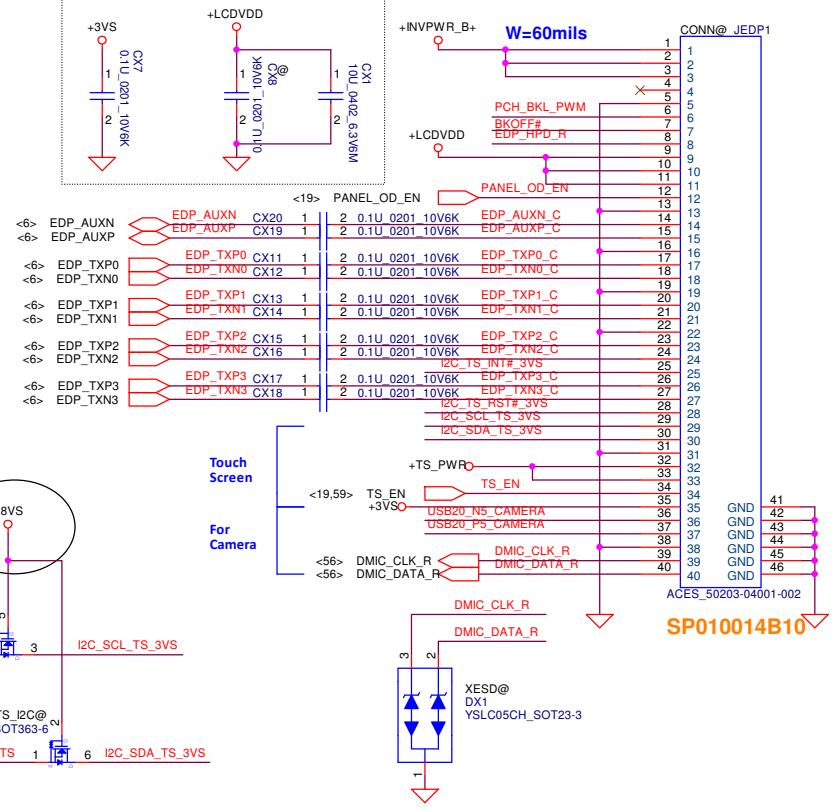
USB/I2C Touch Screen Co-Lay



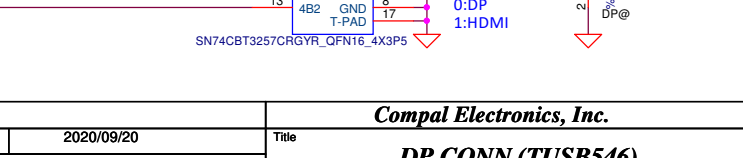
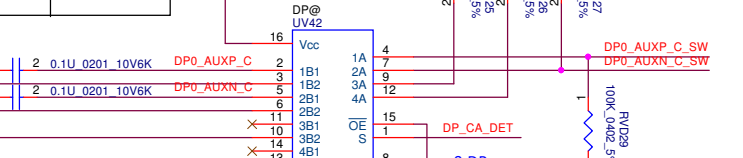
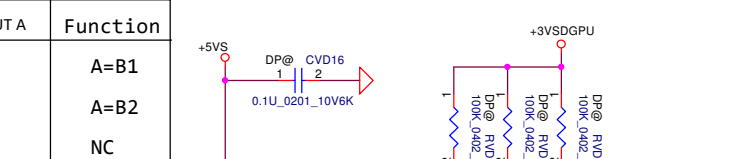
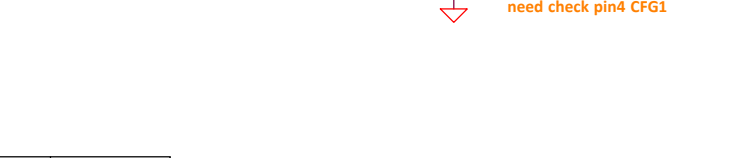
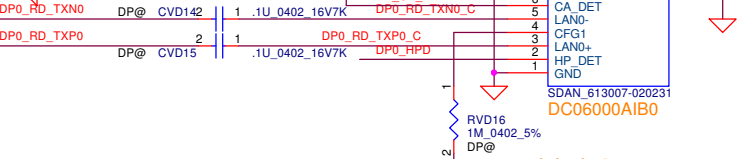
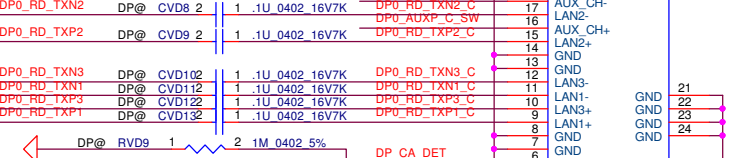
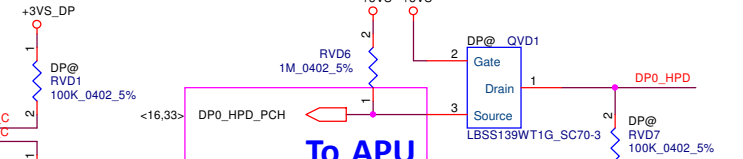
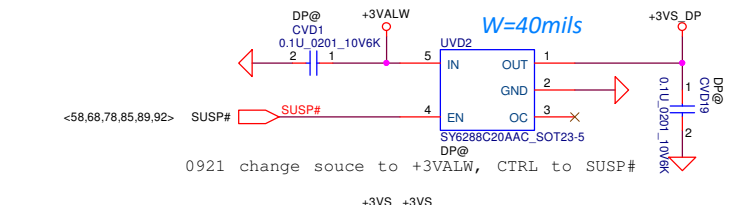
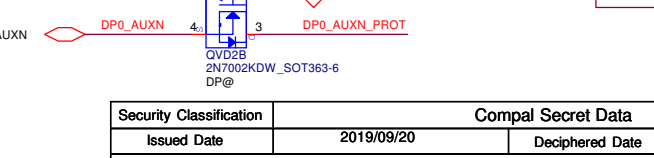
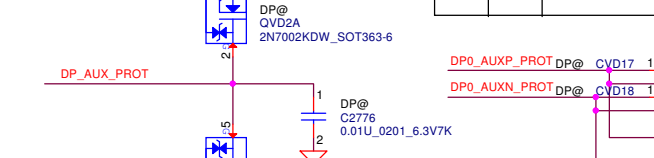
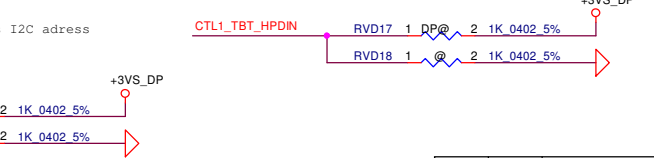
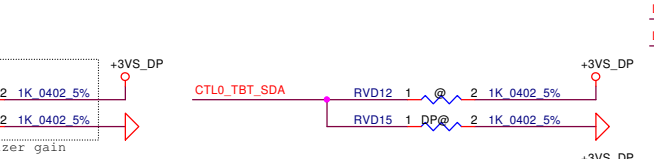
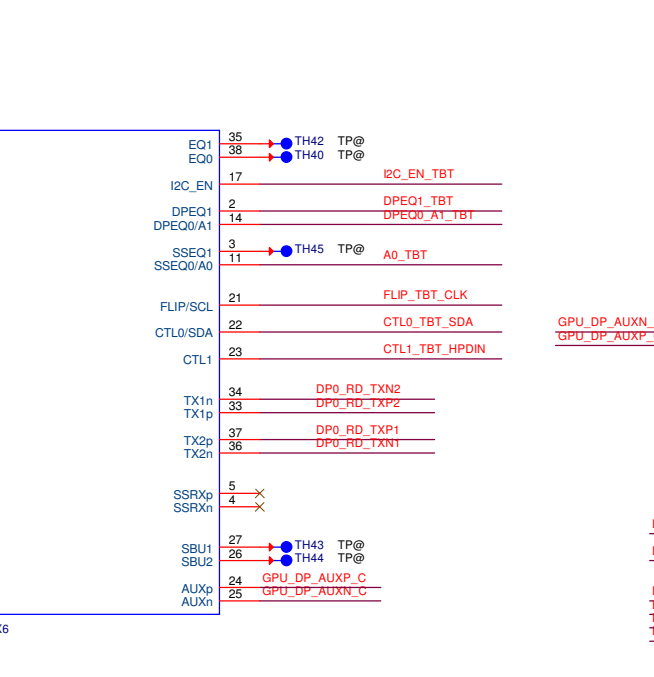
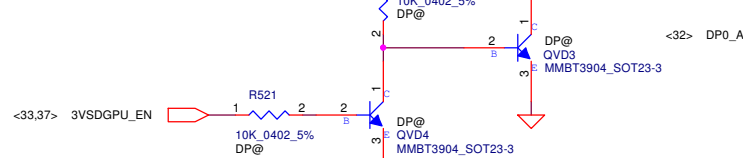
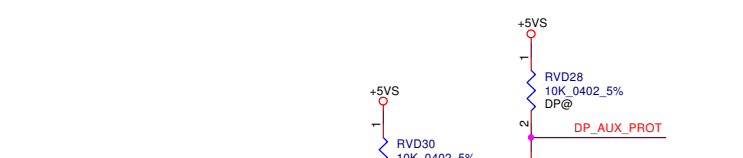
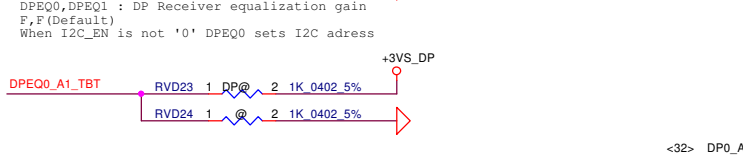
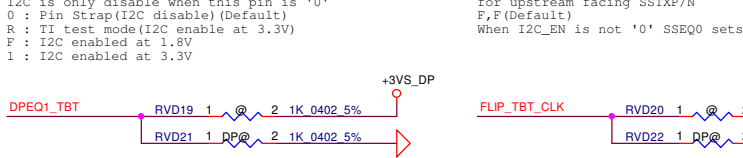
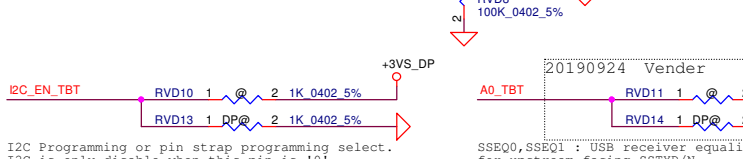
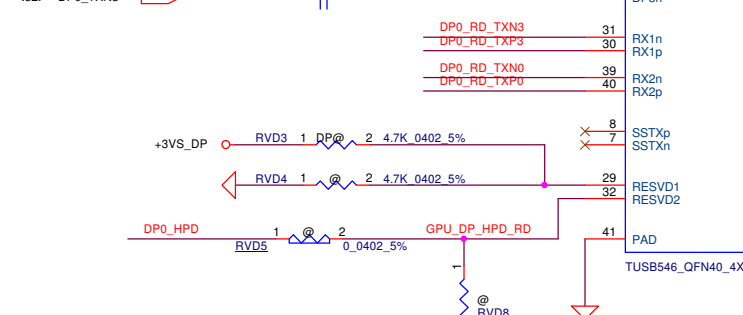
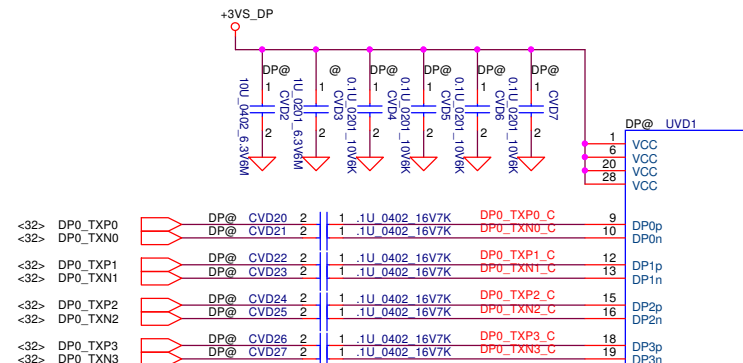
CAMERA



LED PANEL Conn.

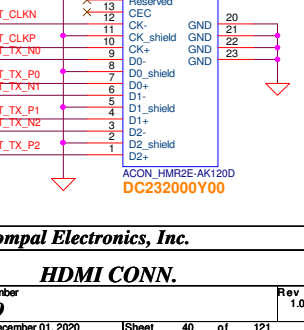
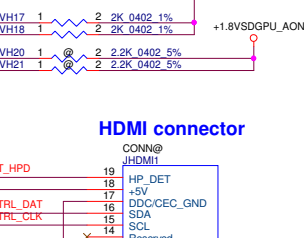
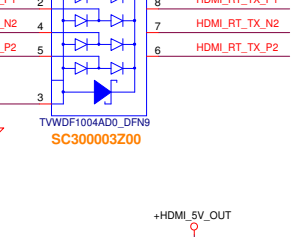
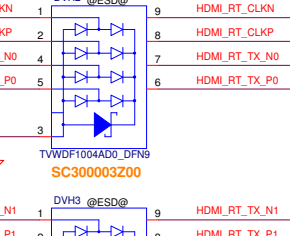
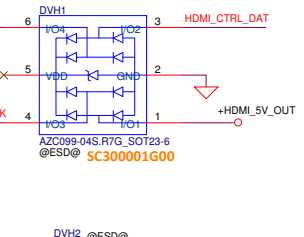
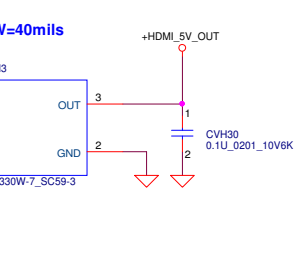
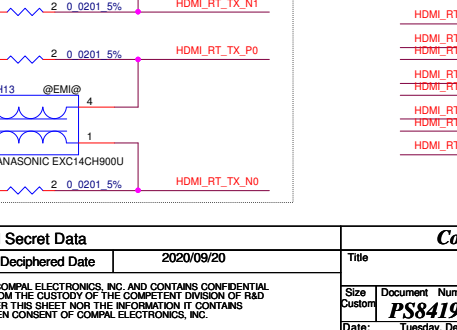
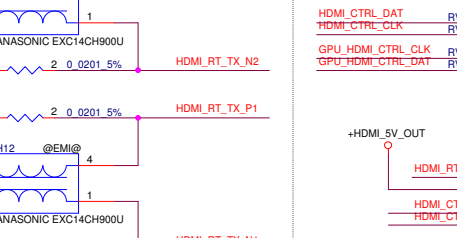
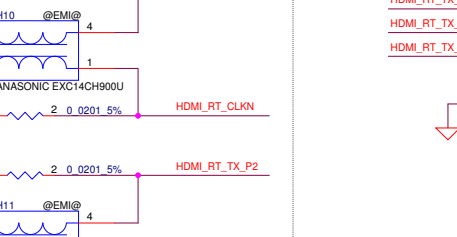
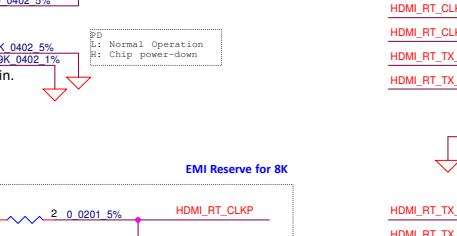
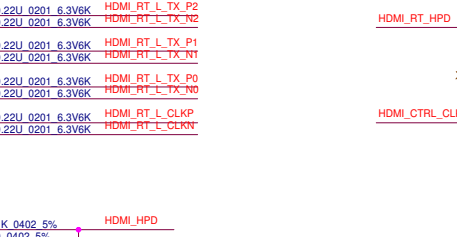
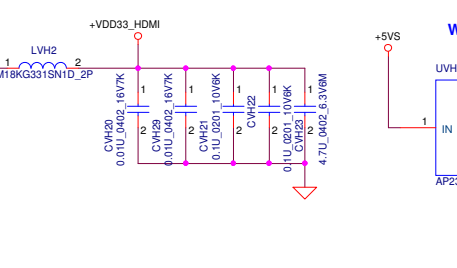
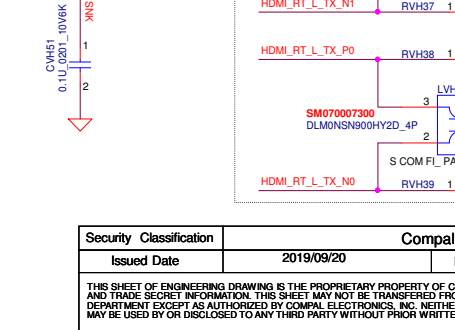
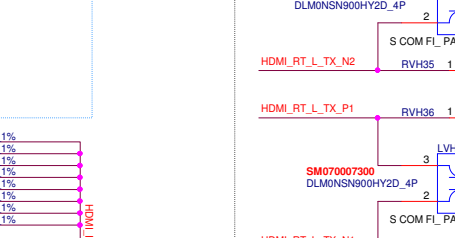
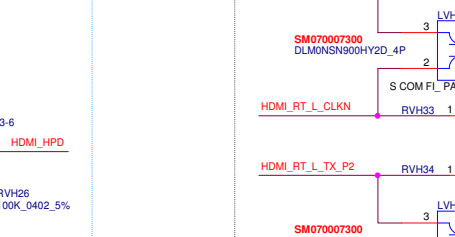
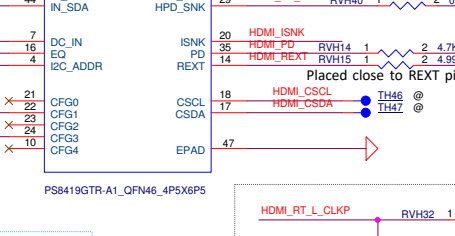
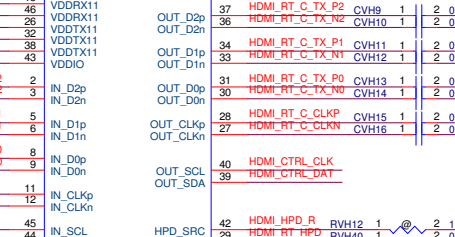
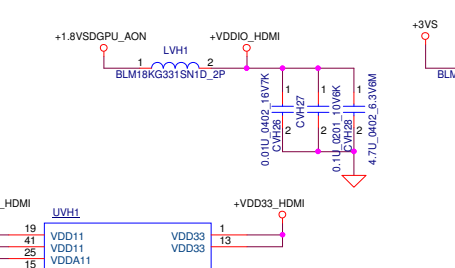
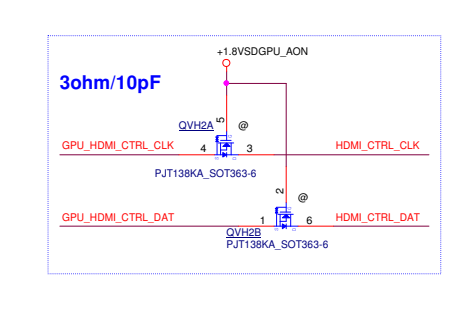
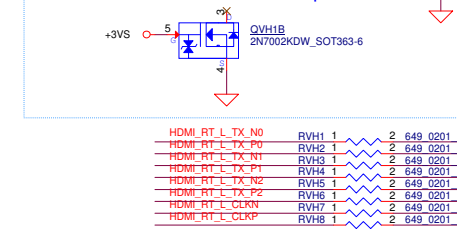
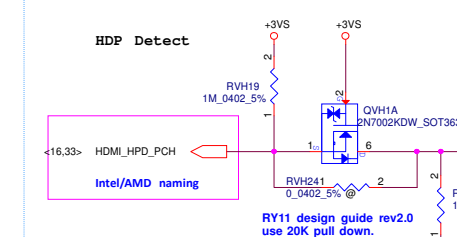
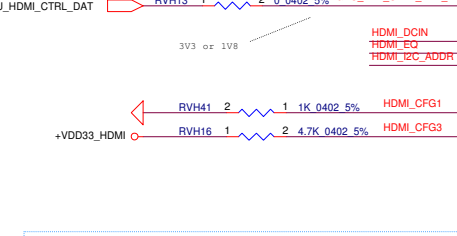
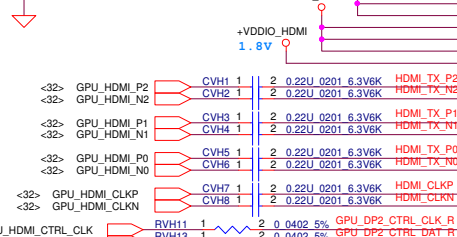
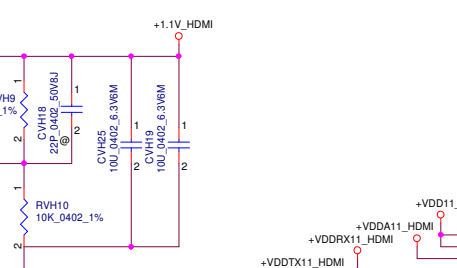
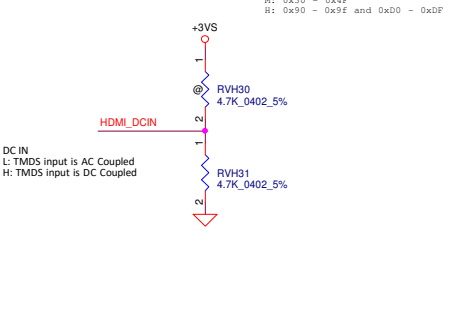
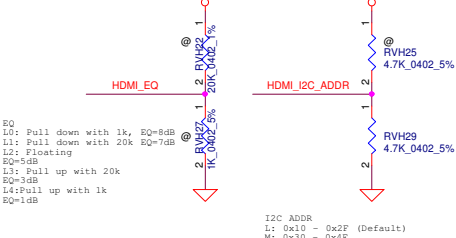
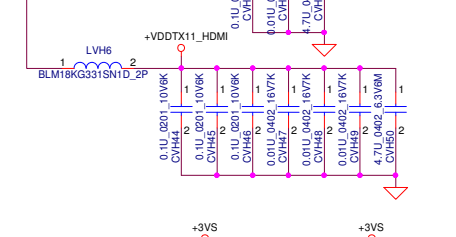
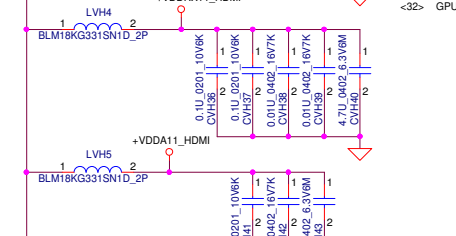
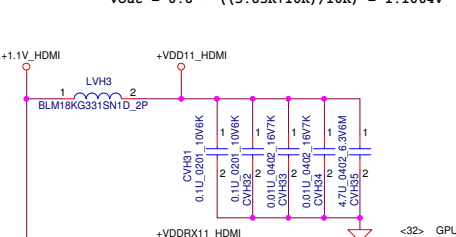
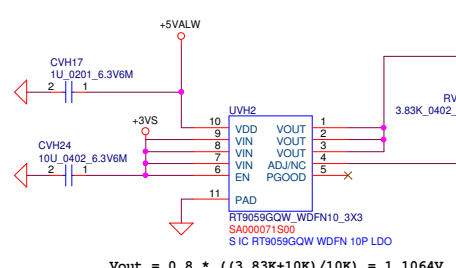
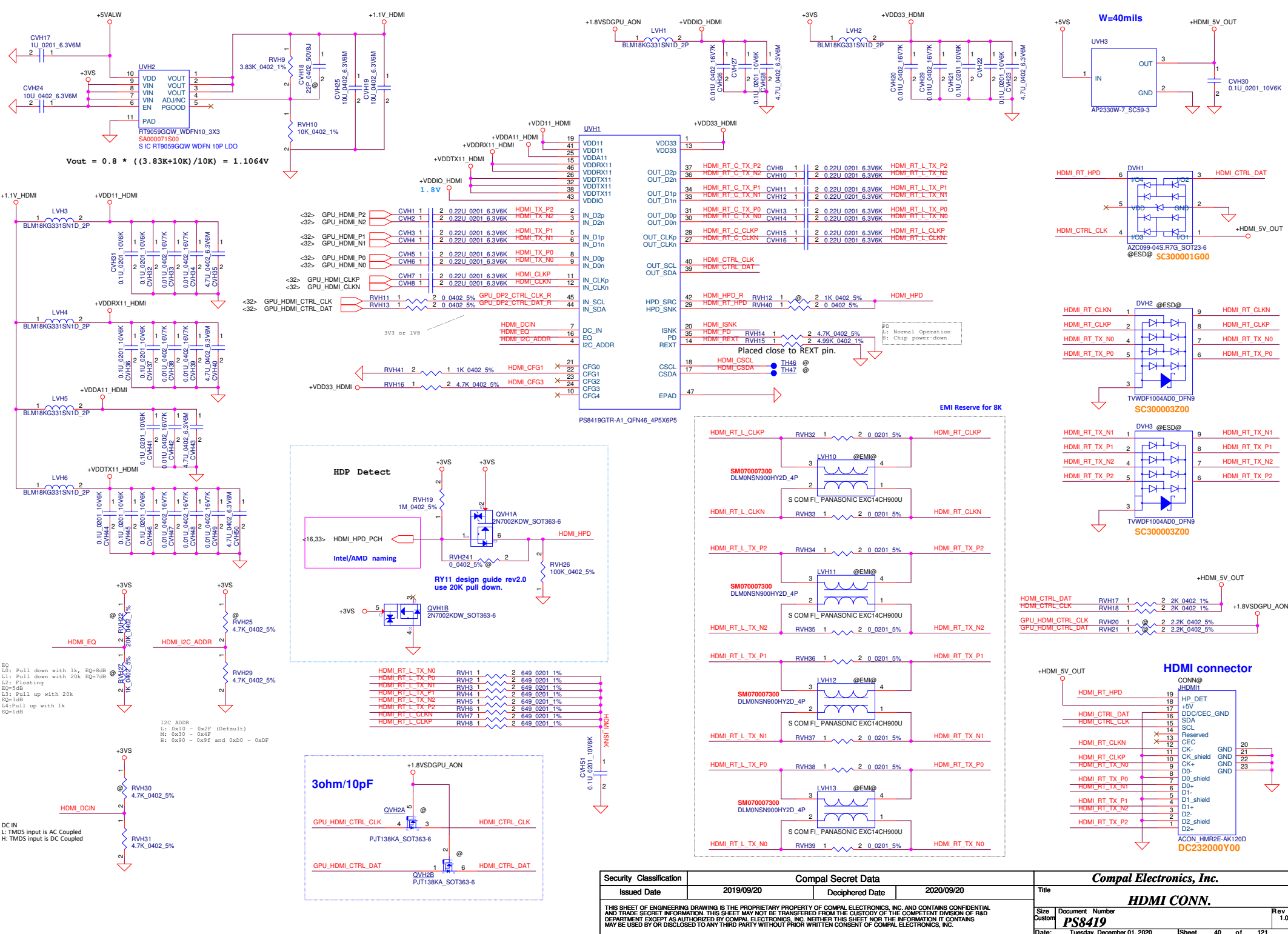


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							Size		Document Number		Rev	
							Custom		FHS1M M/B LA-J871P		1A	
							Date:		Tuesday, December 01, 2020		Sheet 38 of 112	



OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC

Security Classification			Compal Secret Data			Compal Electronics, Inc.		
Issued Date			2019/09/20			Deciphered Date		
2020/09/20			Title			DP CONN (TUSB546)		
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			Custom			LA-K861P		
Date:			Tuesday, December 01, 2020			Sheet 39 of 121		
						Rev 1.0		



EQ: Pull down with 1k, RQ=8dB
L1: Pull down with 20k, RQ=7dB
L2: Floating
EQ=5dB
L3: Pull up with 20k, RQ=3dB
L4: Pull up with 1k, RQ=1dB

I2C ADDR
L: 0x10 - 0x2F (Default)
M: 0x30 - 0x4F
R: 0x90 - 0x9F and 0x00 - 0x0F

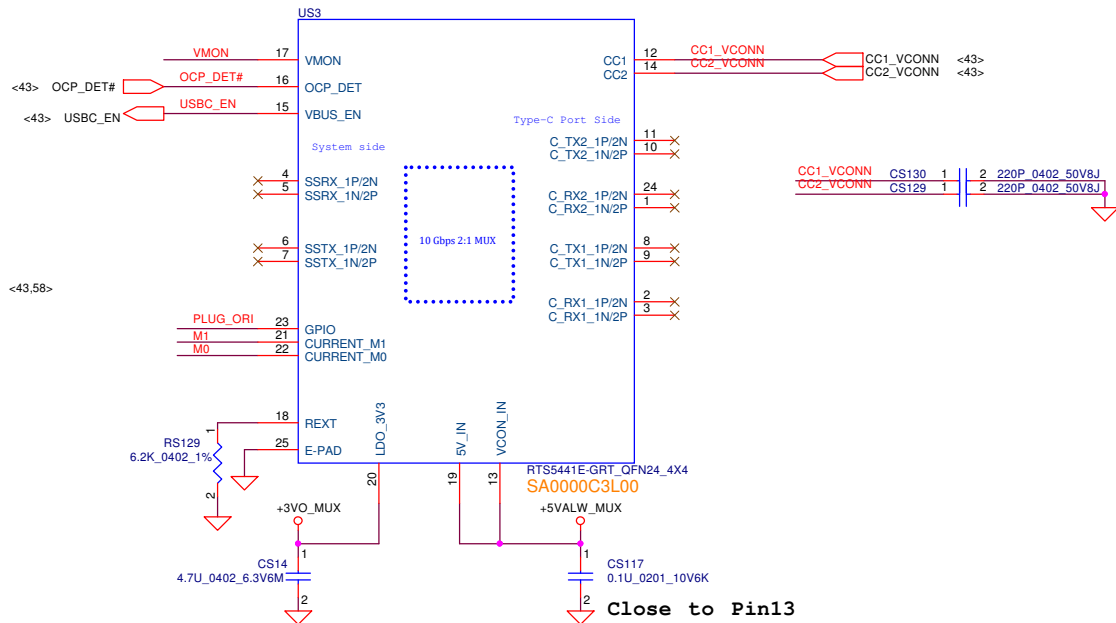
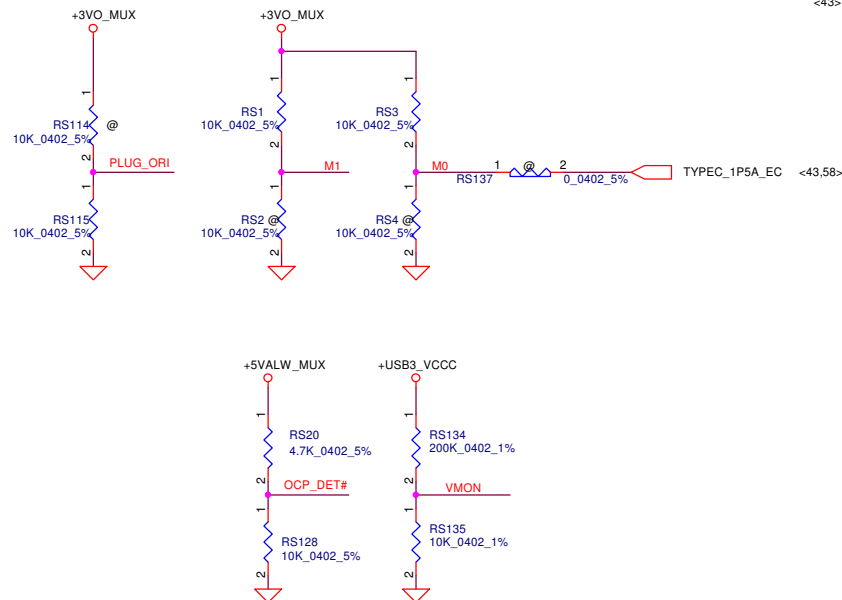
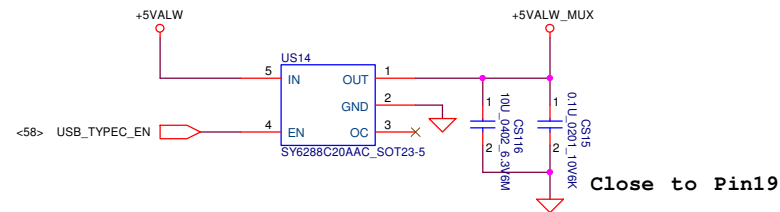
DC IN
L: TMSD input is AC Coupled
H: TMSD input is DC Coupled

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				Sheet 40	of 121

Reserve Page

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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 41 of 112

20191014
- Change to "with no Dual Role support"
- 5441E only uses the function of CC & Power SW



5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

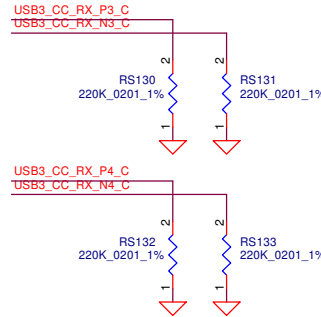
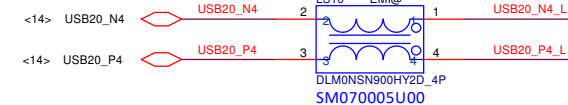
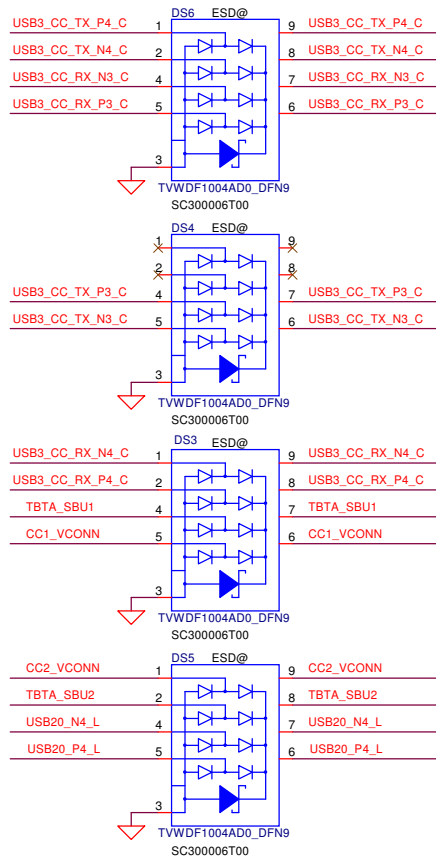
confirm realtek hand-shake			
RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

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				Date: Tuesday, December 01, 2020	
				Sheet 42 of 112	

20191014
 - Change to "with no Dual Role support"
 - CS112/113/114/115 change to 0.33U

20191016
 - USB3 Port5 change to Port3

20191015 - Pin SWAP for layout
 20191016 For ESD request - Gen2 Solution SC300006T00



<42>

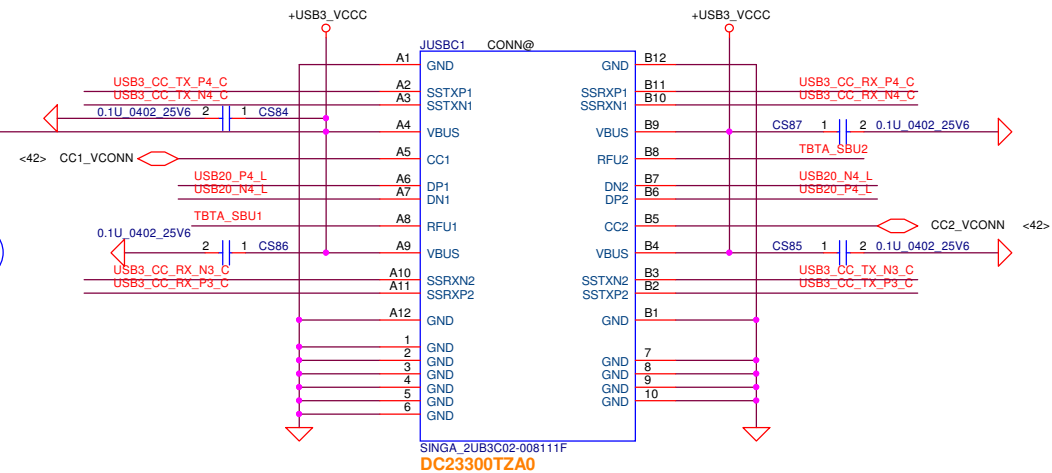
USBC_EN

RB77

47K_0402_5%

G518 MOS Current Limit					
GPP_B1 TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point	
L	L	6.2	0.9A	1.09A	
L	H	3.53	1.5A	1.92A	
H	L	2.54	2A	2.67A	
*H	H	1.94	3A	3.5A	

check bios
 1050 is use PCH output



CC1_VCONN & CC2_VCONN need 20mil trace width.

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				Size Custom	Document Number	Rev 1A
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				Date:	Tuesday, December 01, 2020	Sheet 43 of 112

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				Date:	Tuesday, December 01, 2020	Sheet 44 of 112

Reserve Page

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				Date:	Tuesday, December 01, 2020	Sheet 45 of 112

Reserve Page

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				Date:	Tuesday, December 01, 2020	Sheet 46 of 112

Reserve Page

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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 47 of 112

Reserve Page

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Reserve Page

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				Date:	Tuesday, December 01, 2020	Sheet 49 of 112

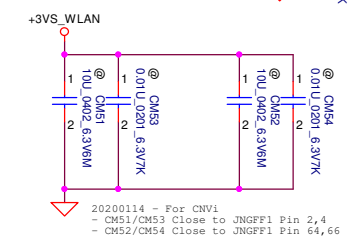
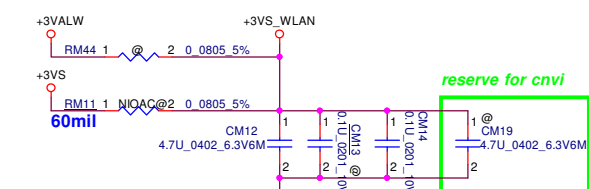
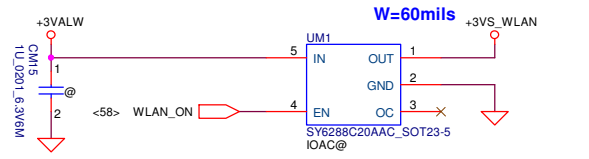
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 50 of 112

20190918
LAN more to IO/B

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Wireless LAN



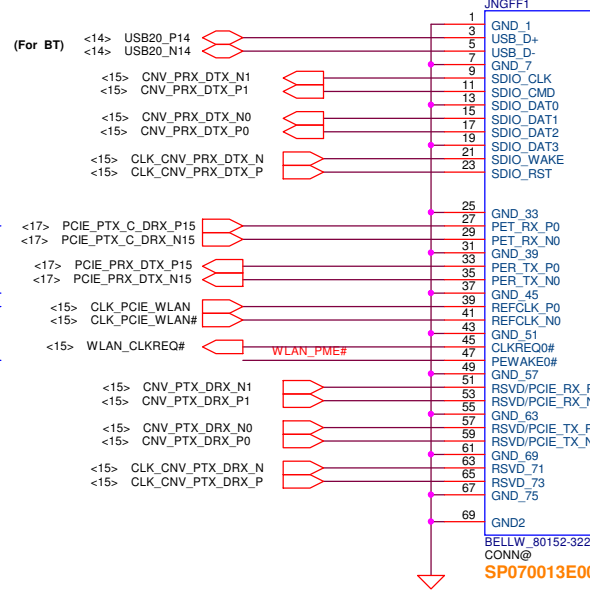
NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO/PERWA#	RESERVED/REFCLKP1	71
68	UM_Power_SM/CLKREQ#	GND	69
66	UM_SWP/PERST#	Reserved/PERP1	67
64	RESERVED	Reserved/PERP1	65
62	ALERT# (IO/0.3V)	GND	63
60	IO CLK (IO/0.3V)	Reserved/PETN1	61
58	IO DATA (IO/0.3V)	Reserved/PETP1	59
56	W_DISABLE#1 (IO/0.3V)	GND	57
54	Reserved/W_DISABLE#2 (IO/0.3V)	PEWAKE# (IO/0.3V)	55
52	PERST# (IO/0.3V)	CLKREQ# (IO/0.3V)	53
50	SUSCLK(32KHz) (IO/0.3V)	GND	51
48	COEX1 (IO/0.1.8V)	REFCLKN0	49
46	COEX2 (IO/0.1.8V)	REFCLKP0	47
44	COEX3 (IO/0.1.8V)	GND	45
42	VENDOR DEFINED	PER#0	43
40	VENDOR DEFINED	PER#0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (IO/0.1.8V)	PET#0	37
34	UART CTS (IO/0.1.8V)	PET#0	35
32	UART Tx (IO/0.1.8V)	GND	33
22	UART Rx (IO/0.1.8V)	SDIO Reset# (IO/0.1.8V)	23
20	UART Wake# (IO/0.3V)	SDIO Wake# (IO/0.1.8V)	21
18	GND	SDIO DAT#0 (IO/0.1.8V)	19
16	LED#2 (IO/0.1.8V)	SDIO DAT#1 (IO/0.1.8V)	17
14	PCM_OUT/ISD_OUT (IO/0.1.8V)	SDIO DAT#2 (IO/0.1.8V)	15
12	PCM_IN/ISD_IN (IO/0.1.8V)	SDIO DAT#3 (IO/0.1.8V)	13
10	PCM_SYNC/ISD_SYNC (IO/0.1.8V)	SDIO CMD (IO/0.1.8V)	11
8	PCM_CLK/ISD_SCK (IO/0.1.8V)	SDIO CLK (IO/0.1.8V)	9
6	LED#1 (IO/0.1.8V)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

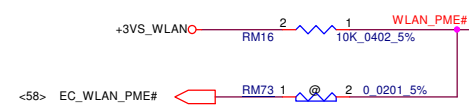
20191210C [FH51M CNVi review]
> RM69 change to 71.5k & CNVi@
> RM70 set CNVi@
> RH22 change to 20K
> RM36/RM37/RM67/RM68 change to 22 ohm
> RM16 recommend to 4.7K (no action)
> RM199 recommend to pop (no action)
> RM45 recommend to 10K (no action)
> WL_OFF# recommend to PU 10K (no action)

20191205 [FH5VF CNVi review]
Pin10 - RM41 Close to PCH
Pin14 - CLKREQ_CNVi# PD RM69(71.5K) (Reserve)
Pin20 - UART_WAKE PU RM70(4.7K) (Reserve)
Pin22 - RM36@M.2 / RH181@PCH
Pin32 - RM37@PCH / RH22@M.2
Pin34 - RM67@M.2 / RH182@PCH
Pin36 - RM68@PCH / RH15@M.2

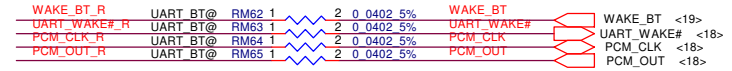
KEY E



(link to PICE Port 3)
PCIE X1
(From PCH CLKOUT2)
PCIE CLK

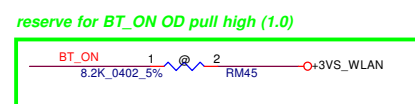
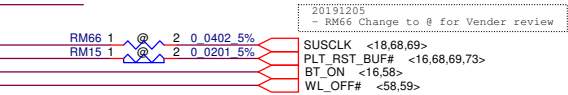
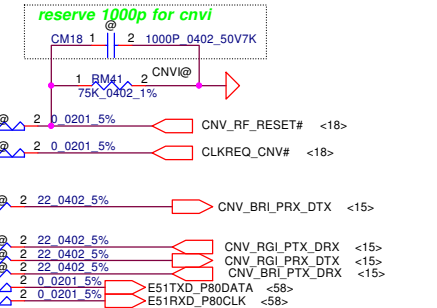
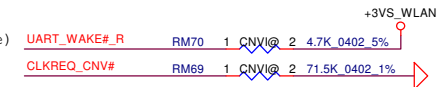
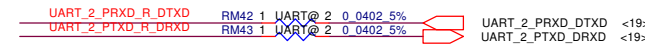


UART BT



20191007
- Add RM62/63/64/65

Co-layout with CNVi for SW debug



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						Rev 1A		
						Date: Tuesday, December 01, 2020		
						Sheet 52 of 112		

Reserve Page

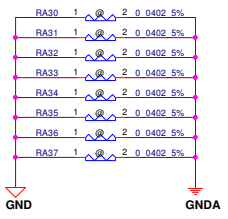
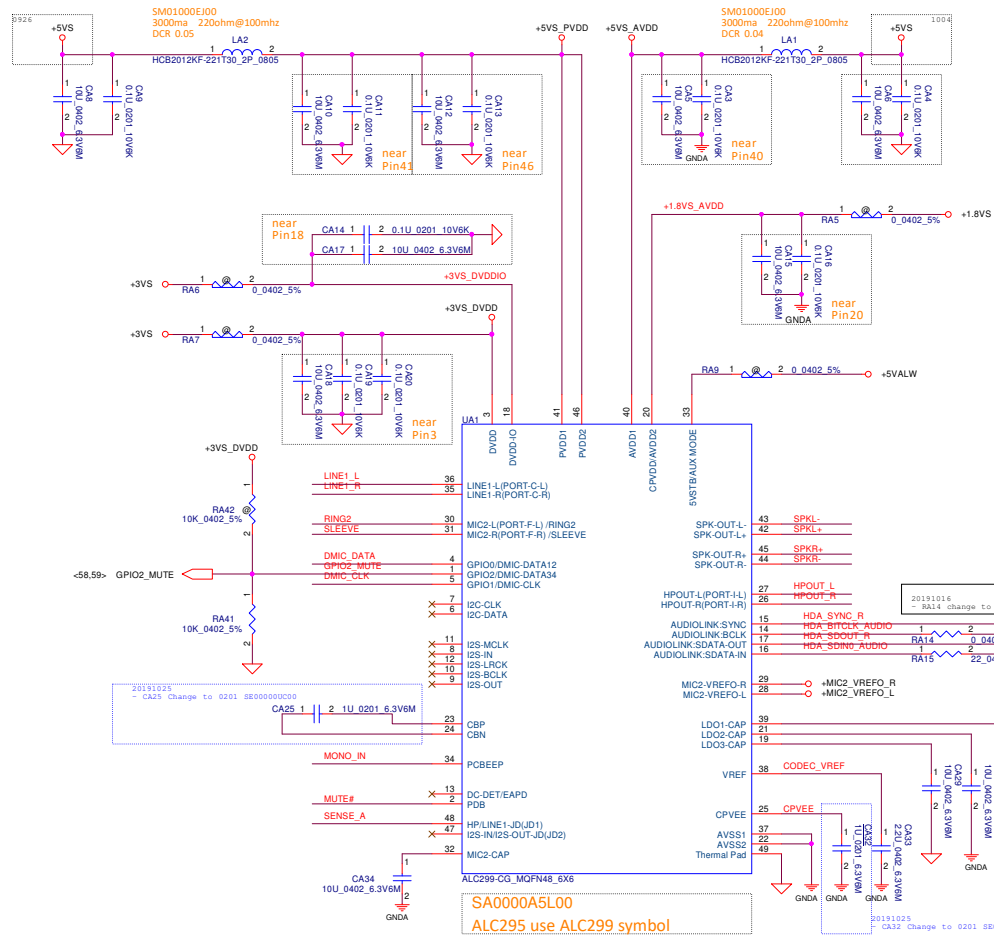
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 53 of 112

Reserve Page

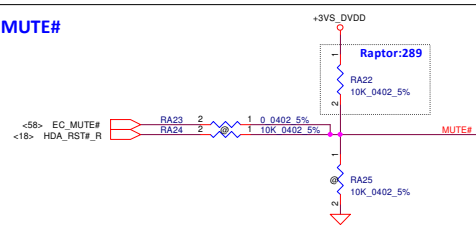
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 54 of 112

Reserve Page

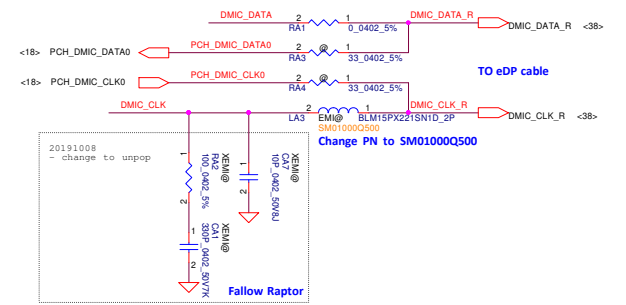
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 55 of 112



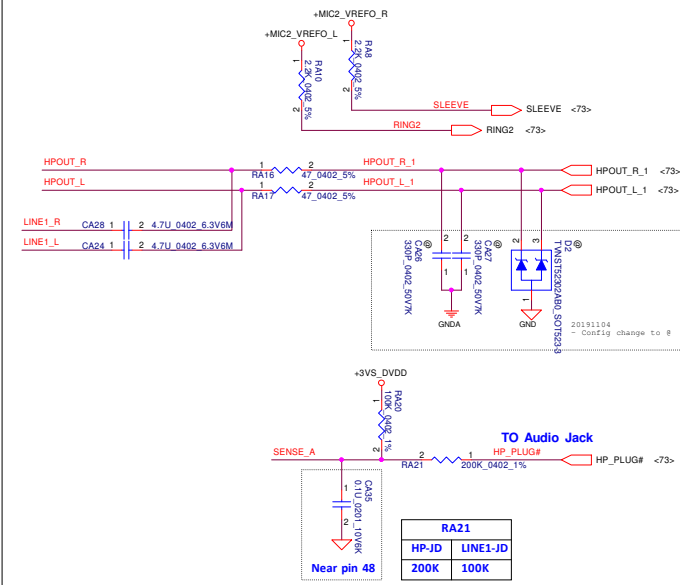
MUTE#



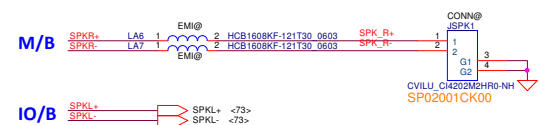
Digital MIC



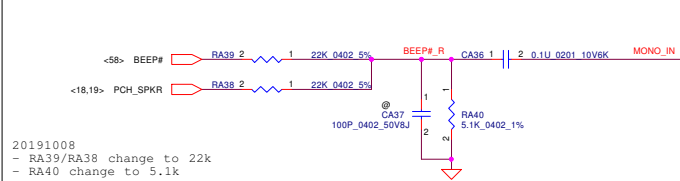
Headphone Out



Speaker



BEEP

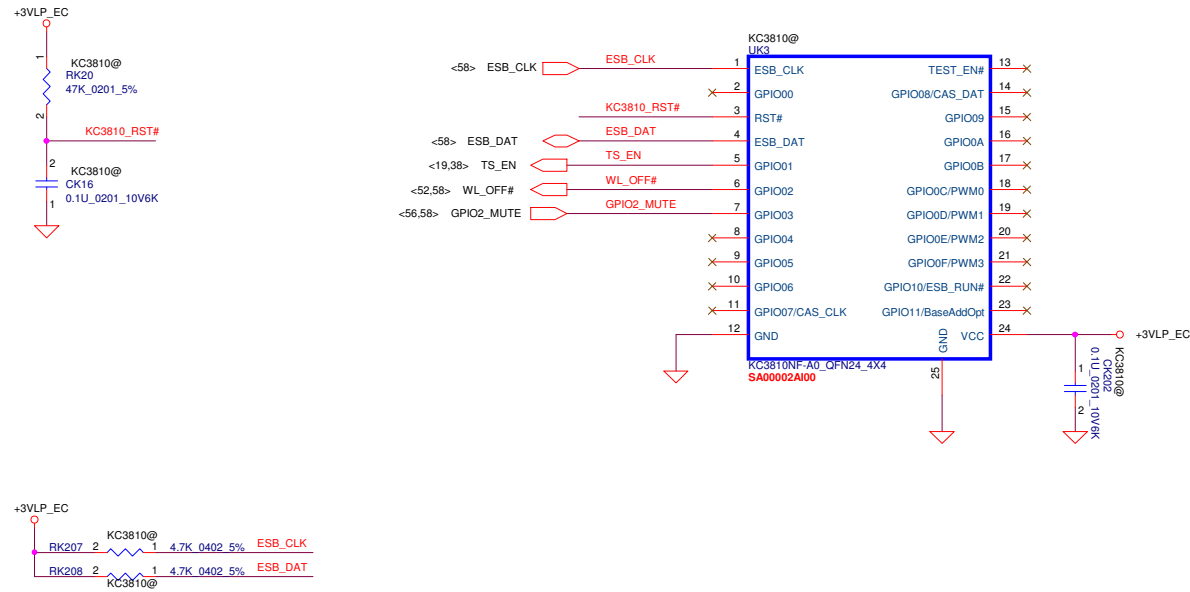


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				Date:	Tuesday, December 01, 2020	Sheet 56 of 112

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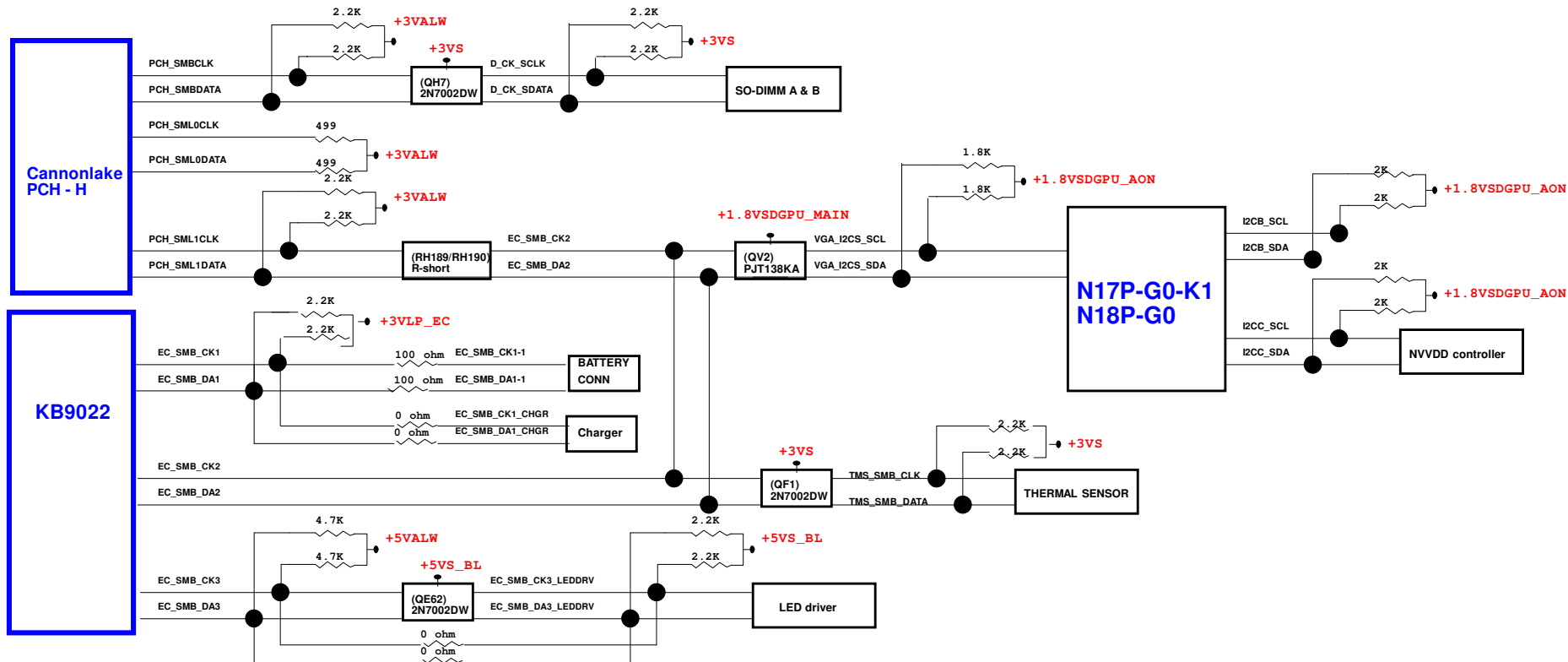
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 57 of 112

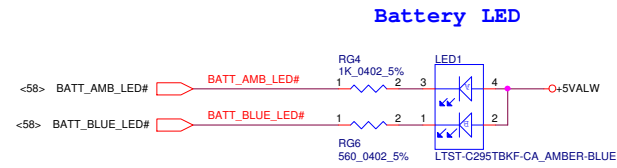
*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.
OMEN New ESB CLK&DAT for Extend I/O



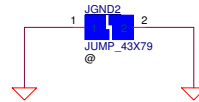
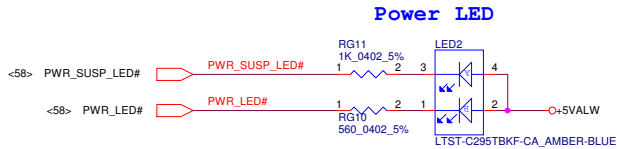
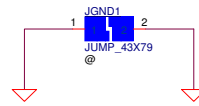
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 60 of 112



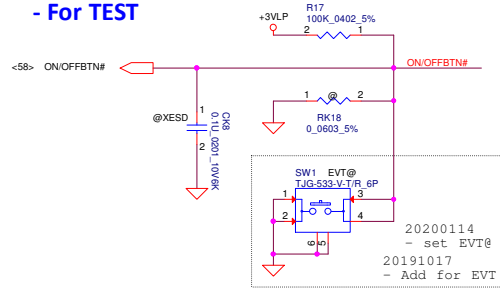


20200211
- RG4/RG11 change to 1k

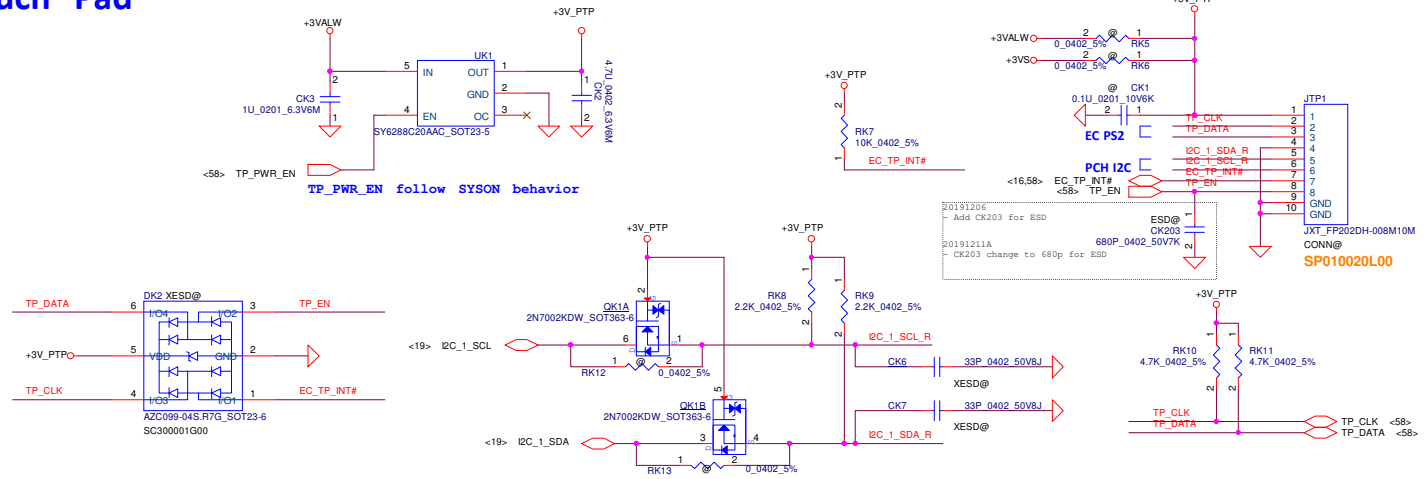


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				FH51M M/B LA-J871P	
				Date:	Rev
				Tuesday, December 01, 2020	1A
				Sheet	62 of 112

ON/OFF BTN - For TEST



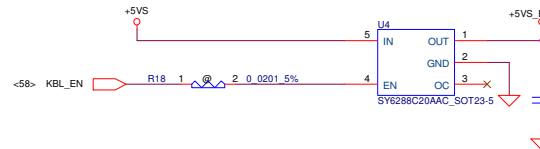
Touch Pad



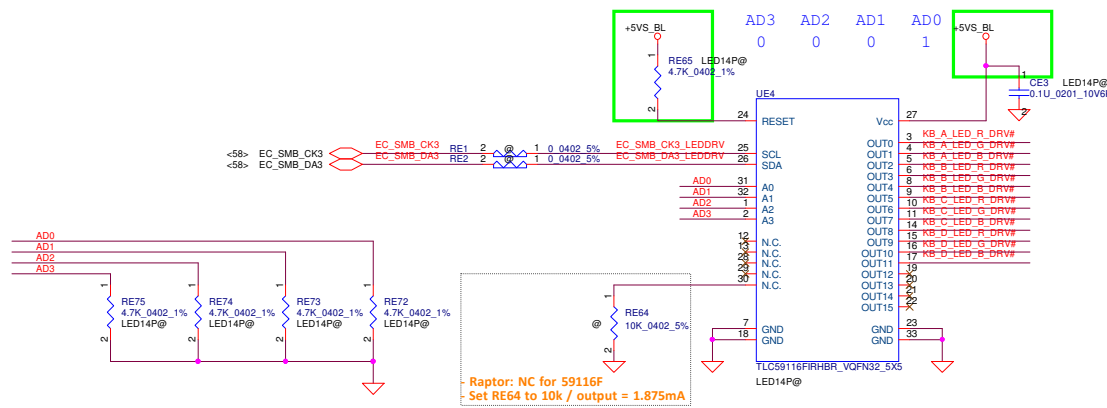
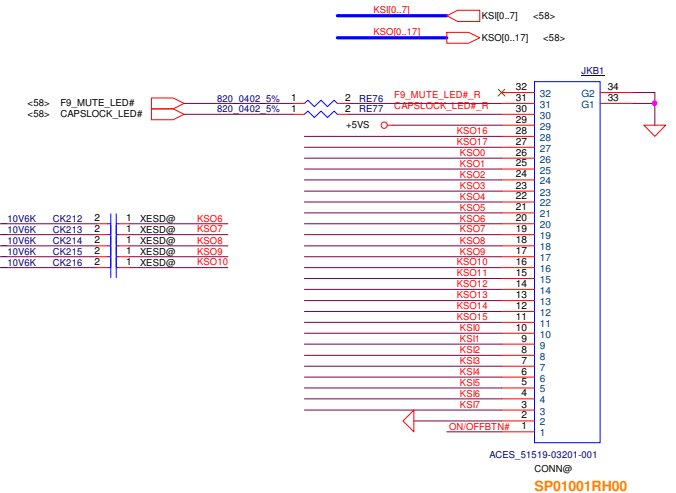
LED driver

20191016
- Remove QE62/RE70/RE69
- PU +5VALW @ EC

20191001
- Change to +5VS only
- KBL_EN only (Check EC Code)
- pop (Normal & RGB)
20200115
- R41/R18 change to R=short



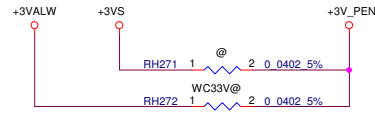
KB Conn. / Backlight



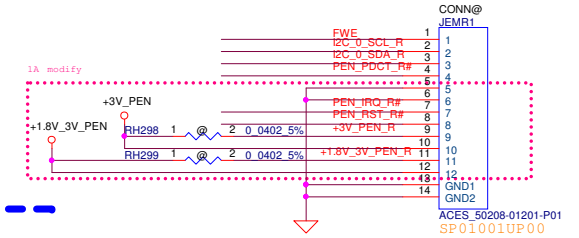
- Raptor: NC for 59116F
- Set RE64 to 10K / output = 1.875mA

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Date: Tuesday, December 01, 2020				Sheet	63 of 112

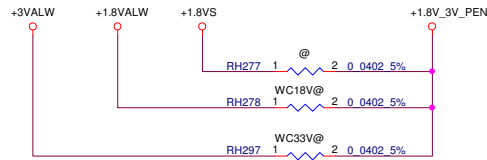
3V_PEN



EMR

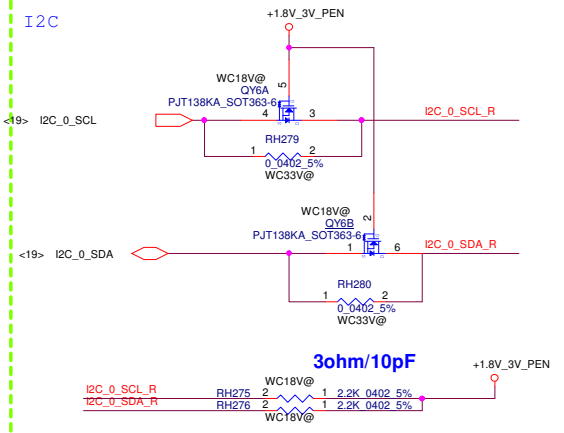


1.8V_PEN

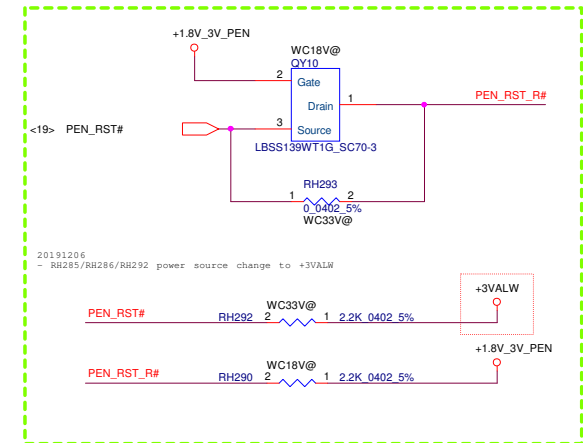
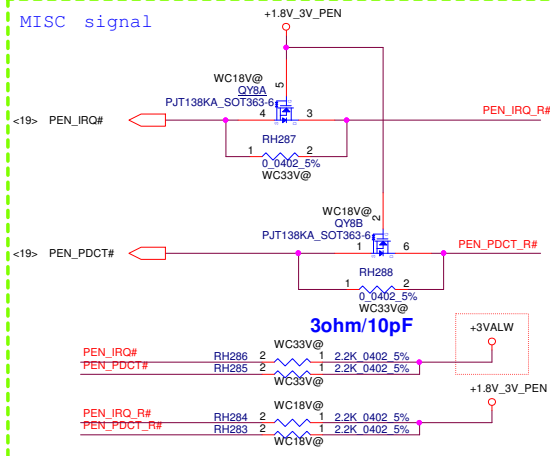


20191008
- QY6/QY8 change to SB000016K00
Default use 0ohm(WC33V@)

I2C



MISC signal

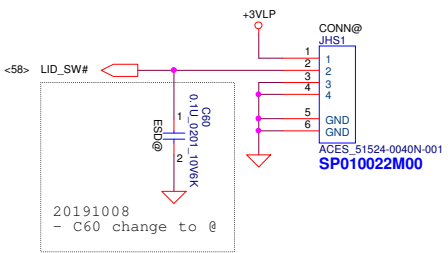


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				Rev 1A	
				Date: Tuesday, December 01, 2020	
				Sheet 64 of 112	

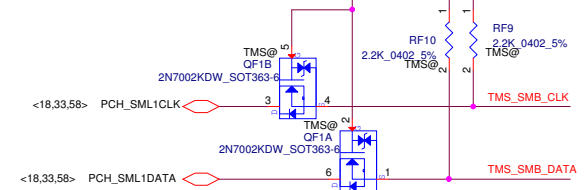
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 65 of 112

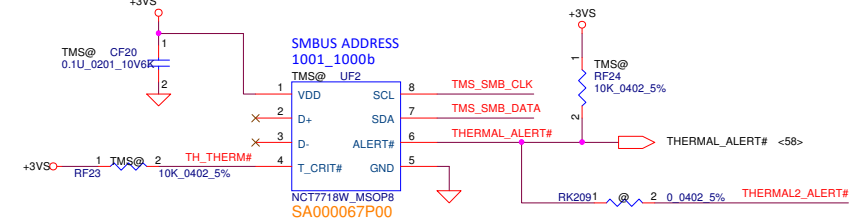
To Hall sensor/B



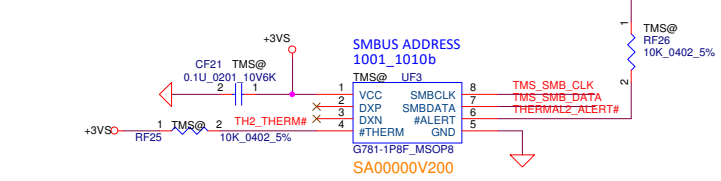
THERMAL SENSOR



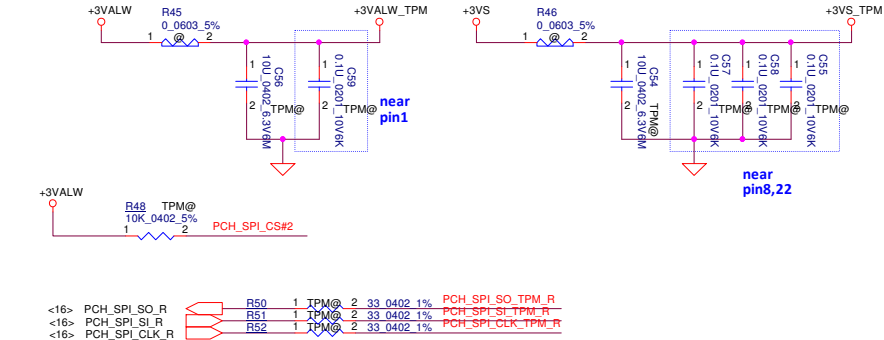
Close to SO-DIMM



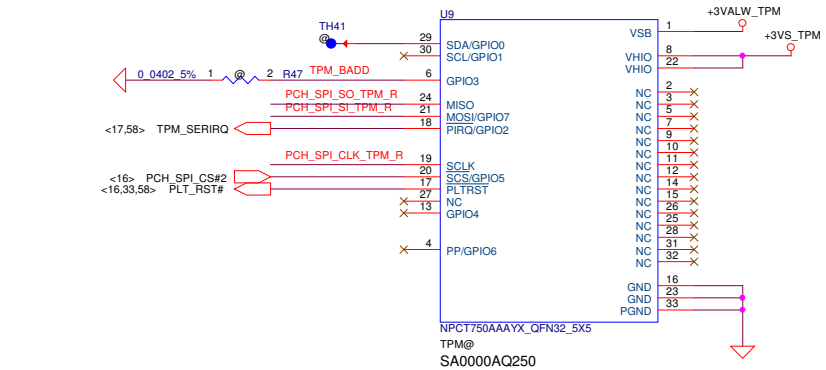
Close to Thermal SKIN



TPM

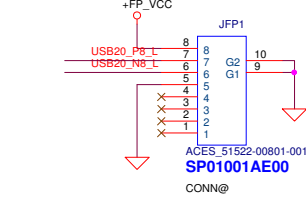
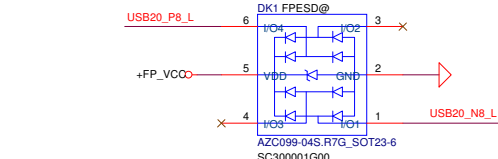
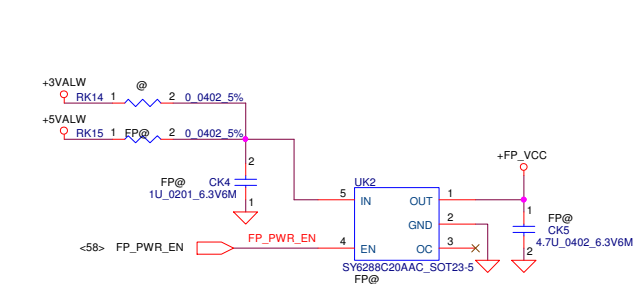


<16>	PCH_SPI_SO_R	R50	1	TPM@	2	33	0402	1%	PCH_SPI_SO_TPM_R
<16>	PCH_SPI_SL_R	R51	1	TPM@	2	33	0402	1%	PCH_SPI_SL_TPM_R
<16>	PCH_SPI_CLK_R	R52	1	TPM@	2	33	0402	1%	PCH_SPI_CLK_TPM_R

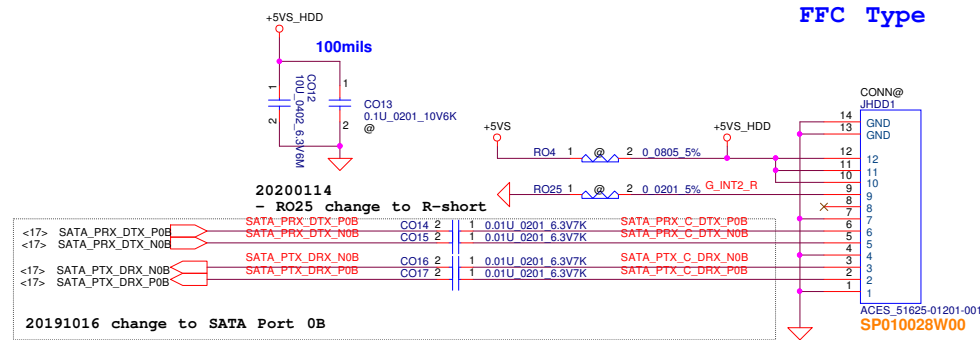


SA0000AQ250, S IC NPCT750AABYX QFN 32P TPM

Finger Print



PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC

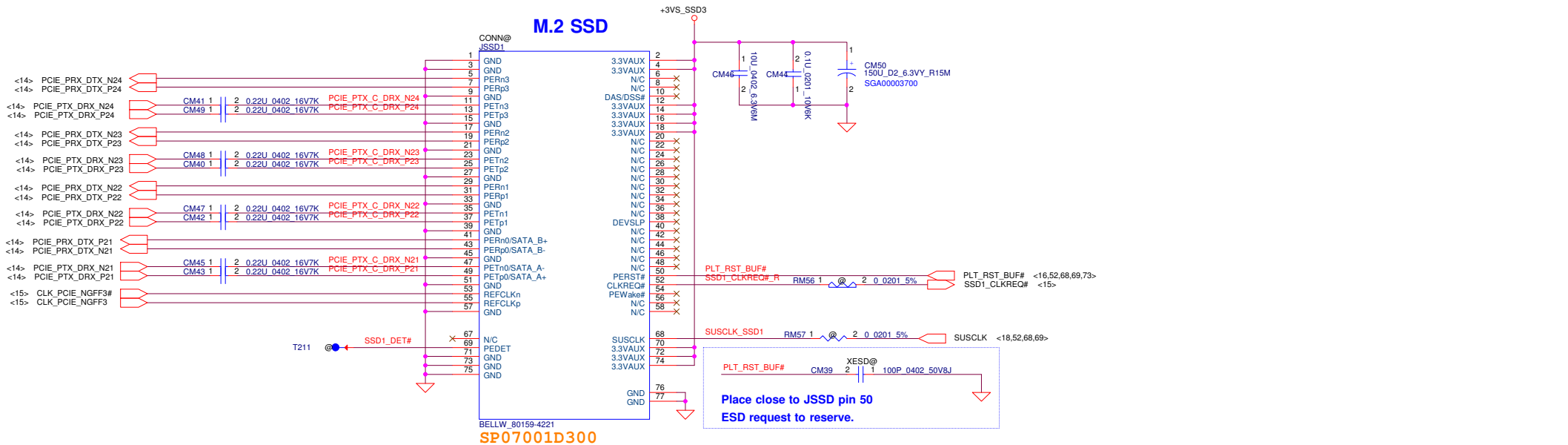
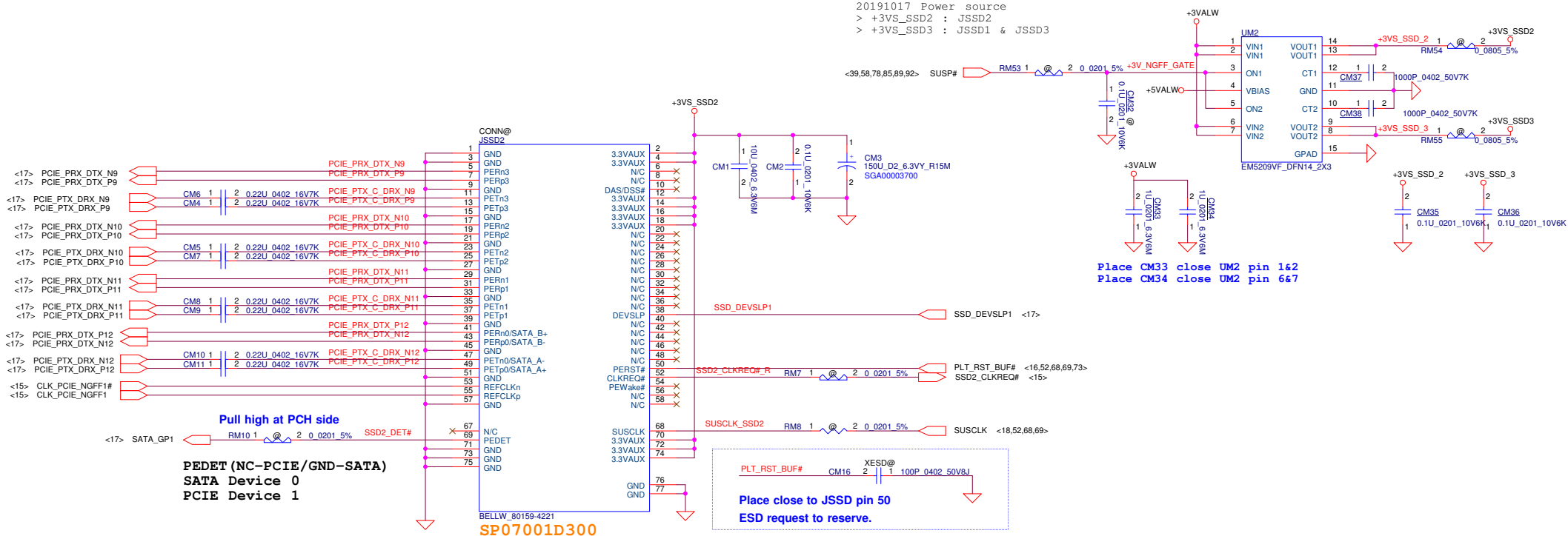


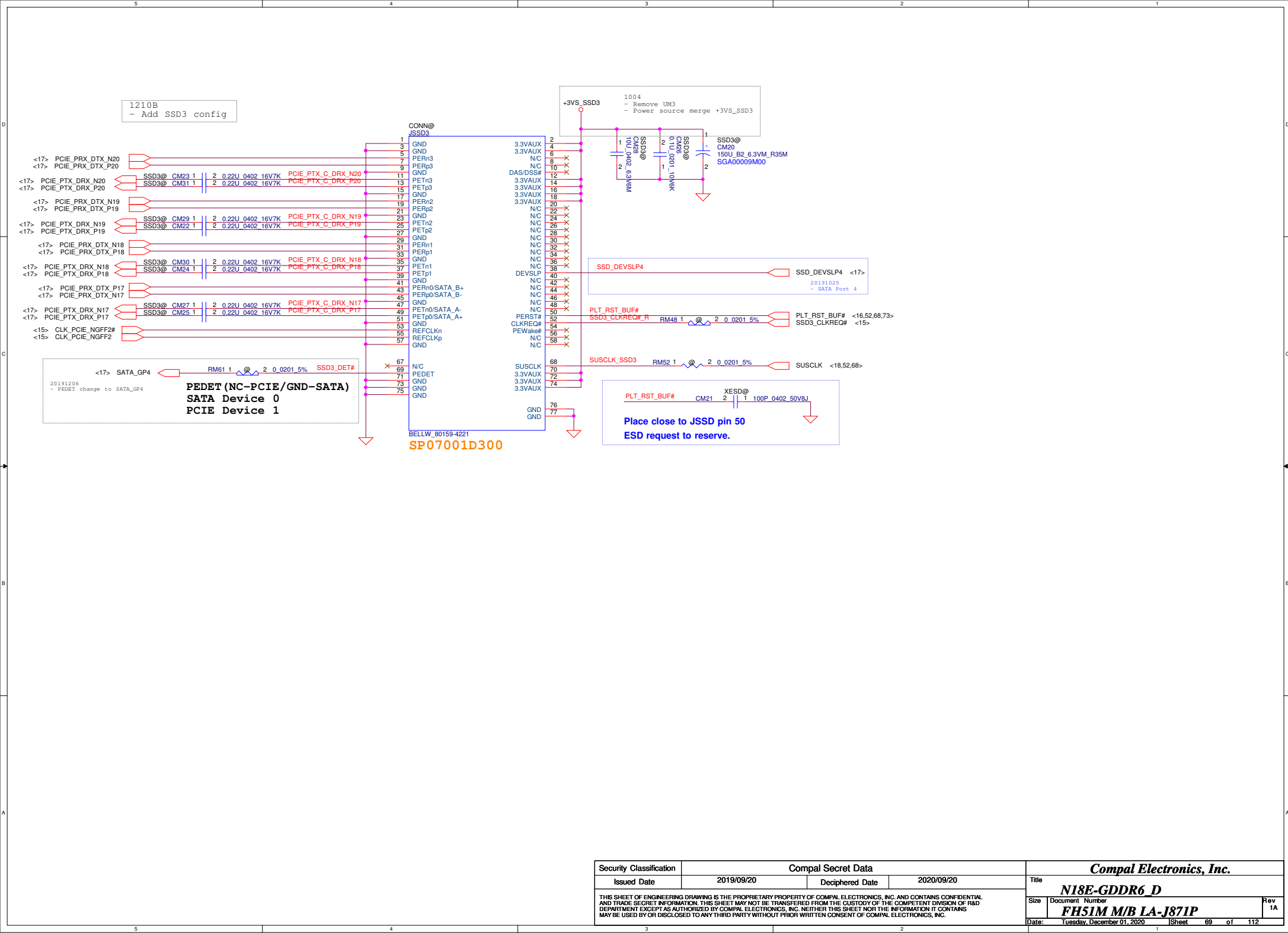
20190918

Remove HDD Re-driver

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Date: Tuesday, December 01, 2020				Sheet	Rev 1A
				67 of 112	

20191017 Power source
> +3VS_SSD2 : JSSD2
> +3VS_SSD3 : JSSD1 & JSSD3

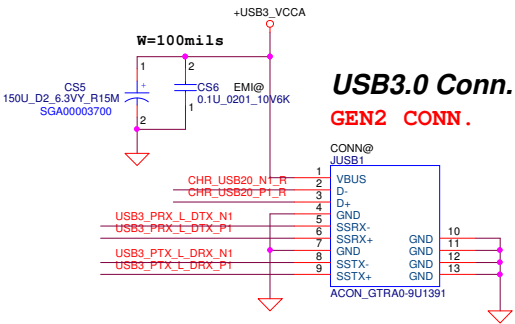
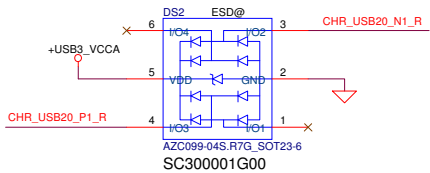
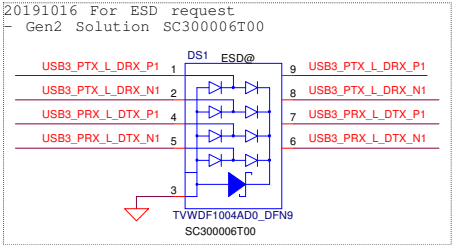
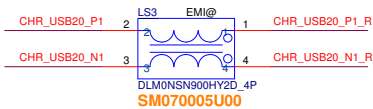
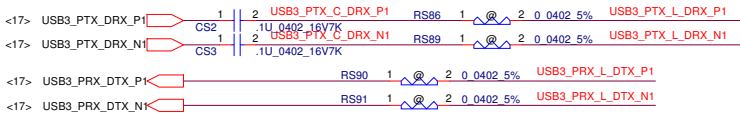




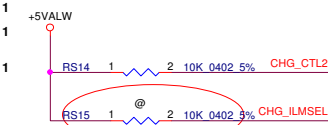
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 70 of 112

USB3.0



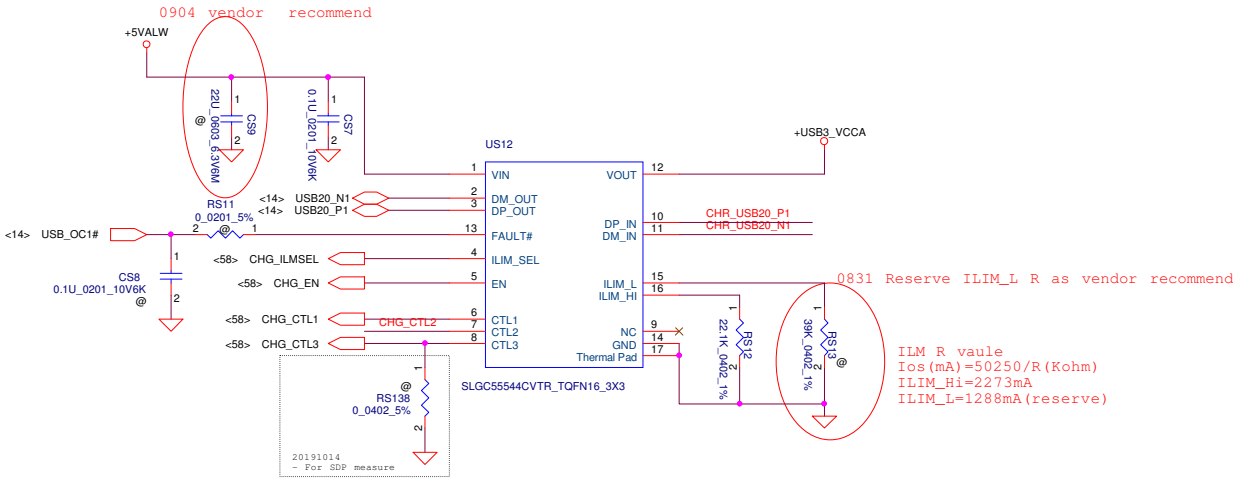
USB Host Charger



0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	1	0	1		SDP1-OFF	ILIM_H		Port power off
0	1	0	1		SDP1	ILIM_H		Data Lines Connected
0	1	1	1		DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1		CDP	ILIM_H		Data Lines Connected

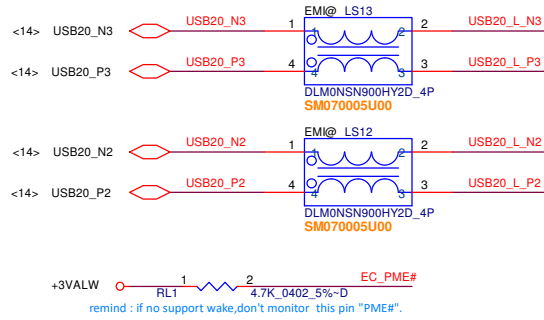


20190918

USB3 Port3 move to IO/B

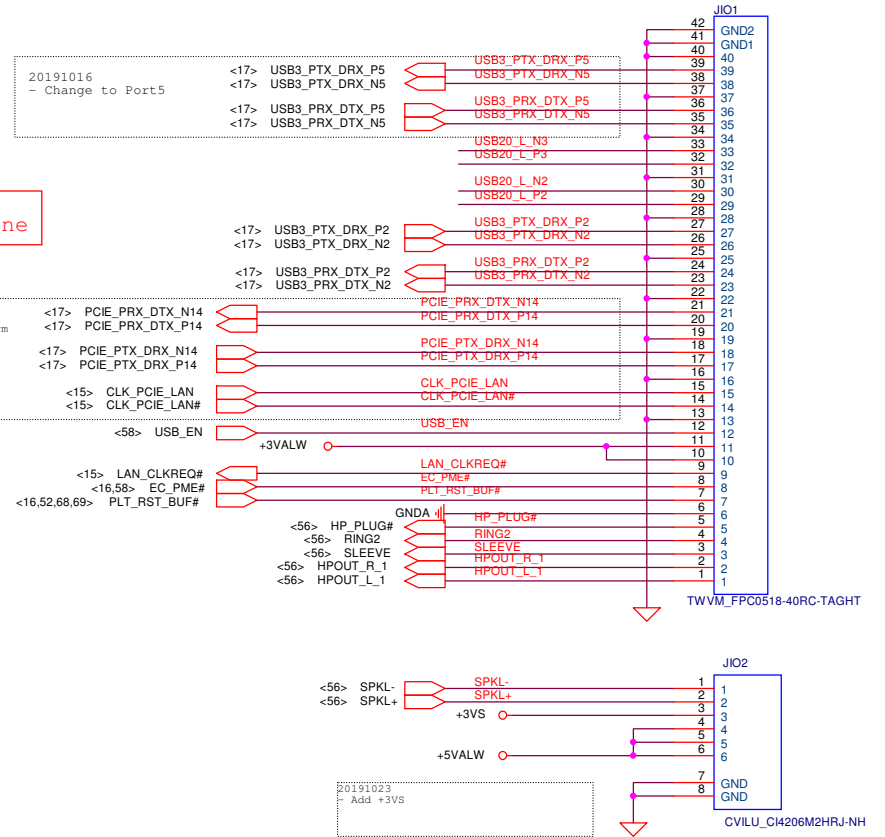
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 72 of 112

IO/B CONN



1209A
- IO_B change pin define

20191008
- LAN PCIe&CLK Remove AC Cap > Vender confirm
(CL136/137/138/139)



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								IO/B LAN E2600			
								Size		Document Number	
								Custom		FHS1M M/B LA-J871P	
								Date:		Tuesday, December 01, 2020	
								Sheet		73 of 112	
								Rev		1A	

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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 74 of 112

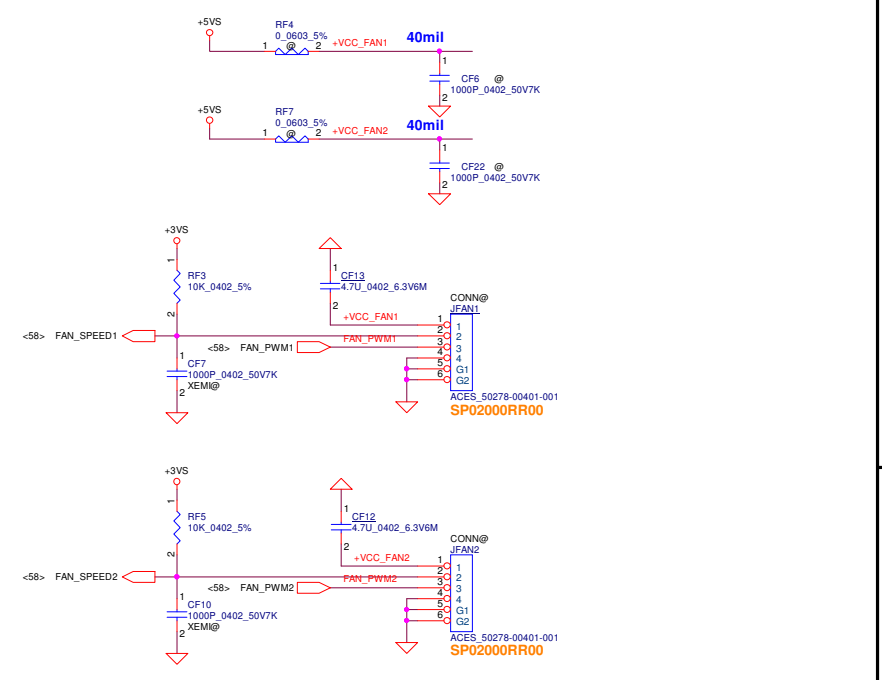
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 75 of 112

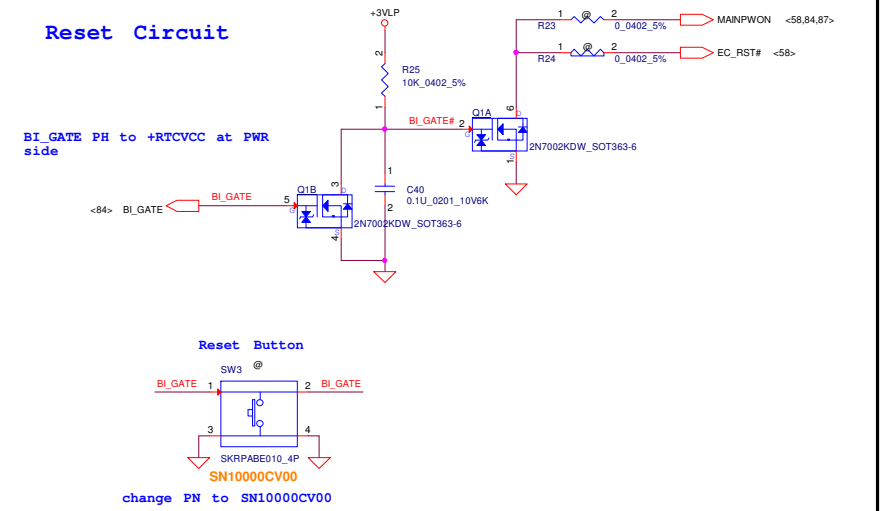
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 76 of 112

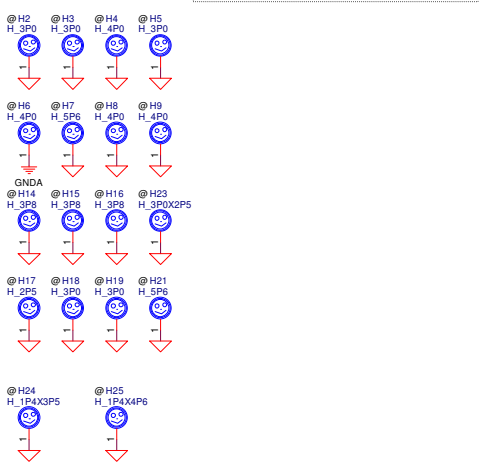
FAN Conn



Reset Circuit



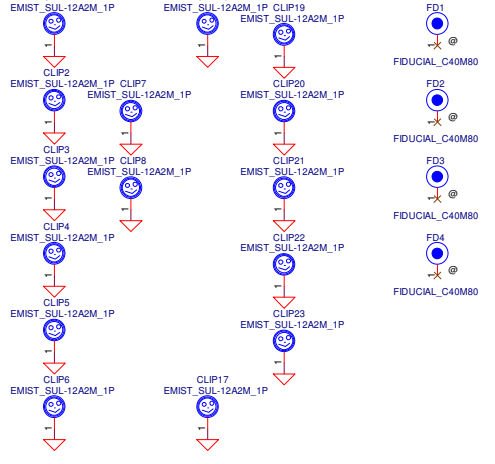
Screw Hole



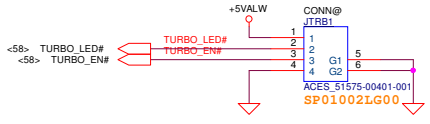
Stand Off



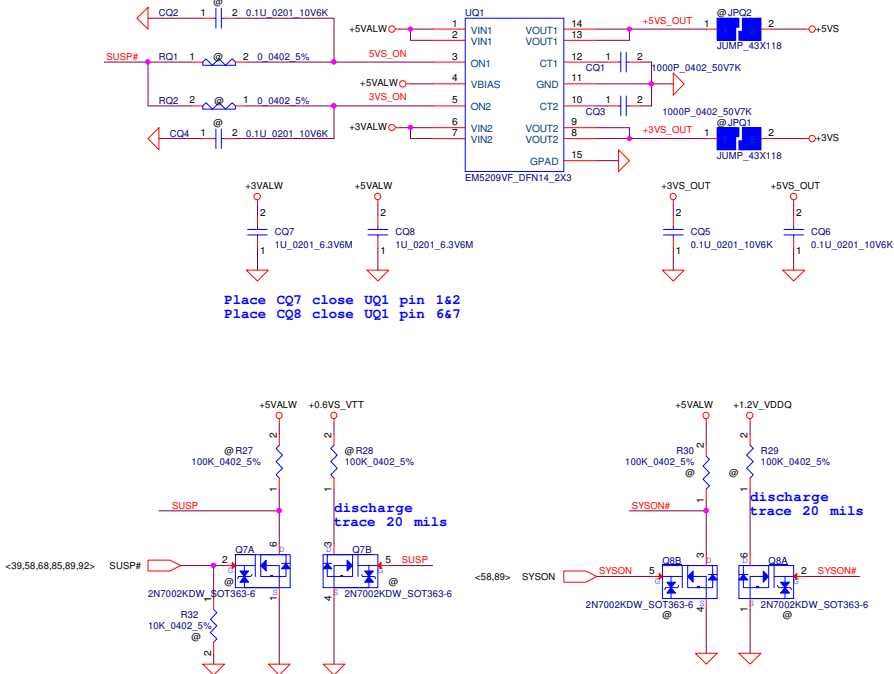
Clips



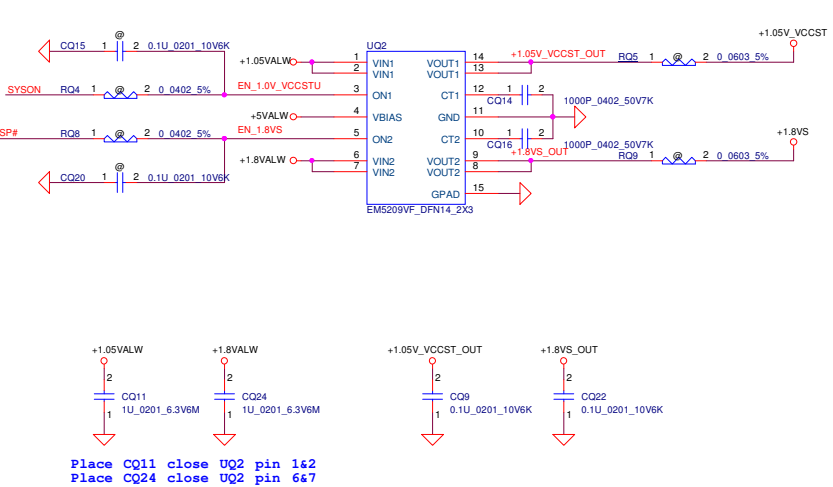
Turbo Key



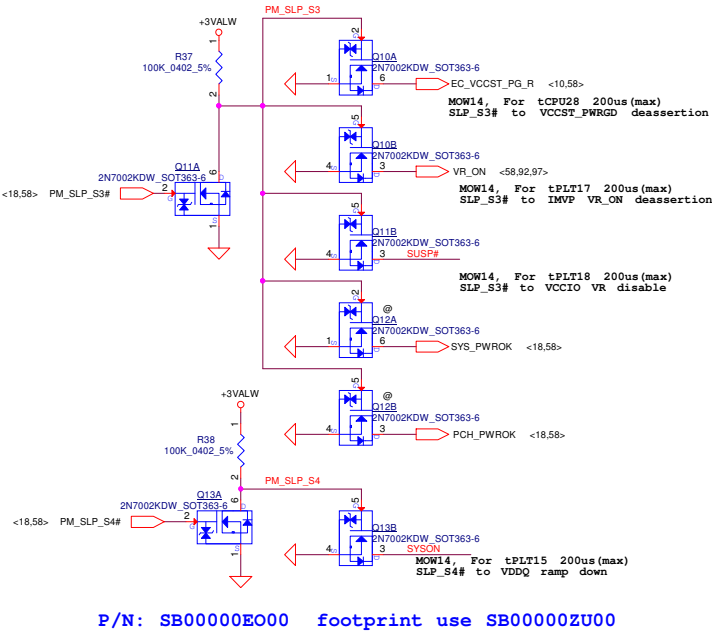
System DC interface



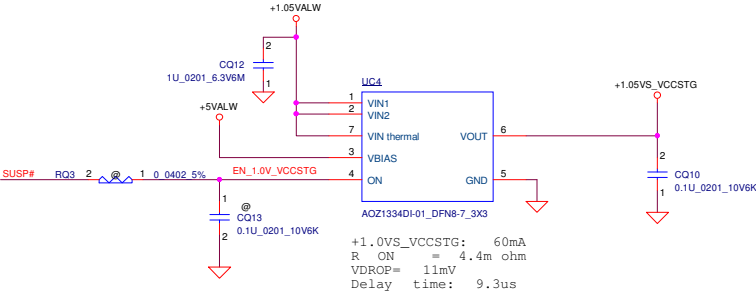
+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



For Power ON/Off Sequence



+1.05VALW TO +1.05VS_VCCSTG



Reserve Page

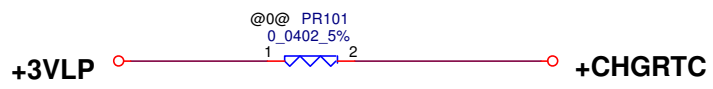
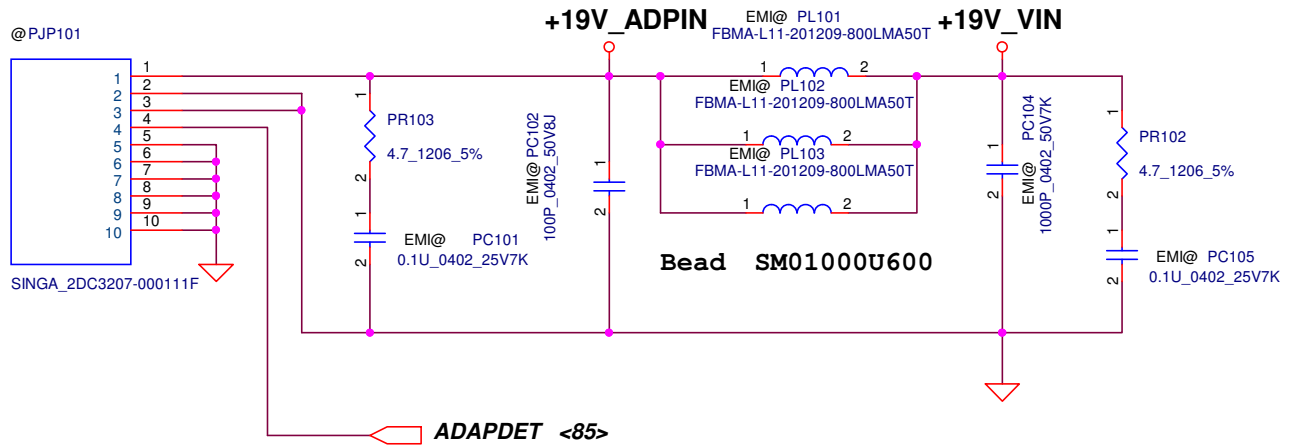
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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 79 of 112

Reserve Page

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					FH51M M/B LA-J871P	1A
				Date:	Tuesday, December 01, 2020	Sheet 80 of 112

Reserve Page

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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 61 of 121



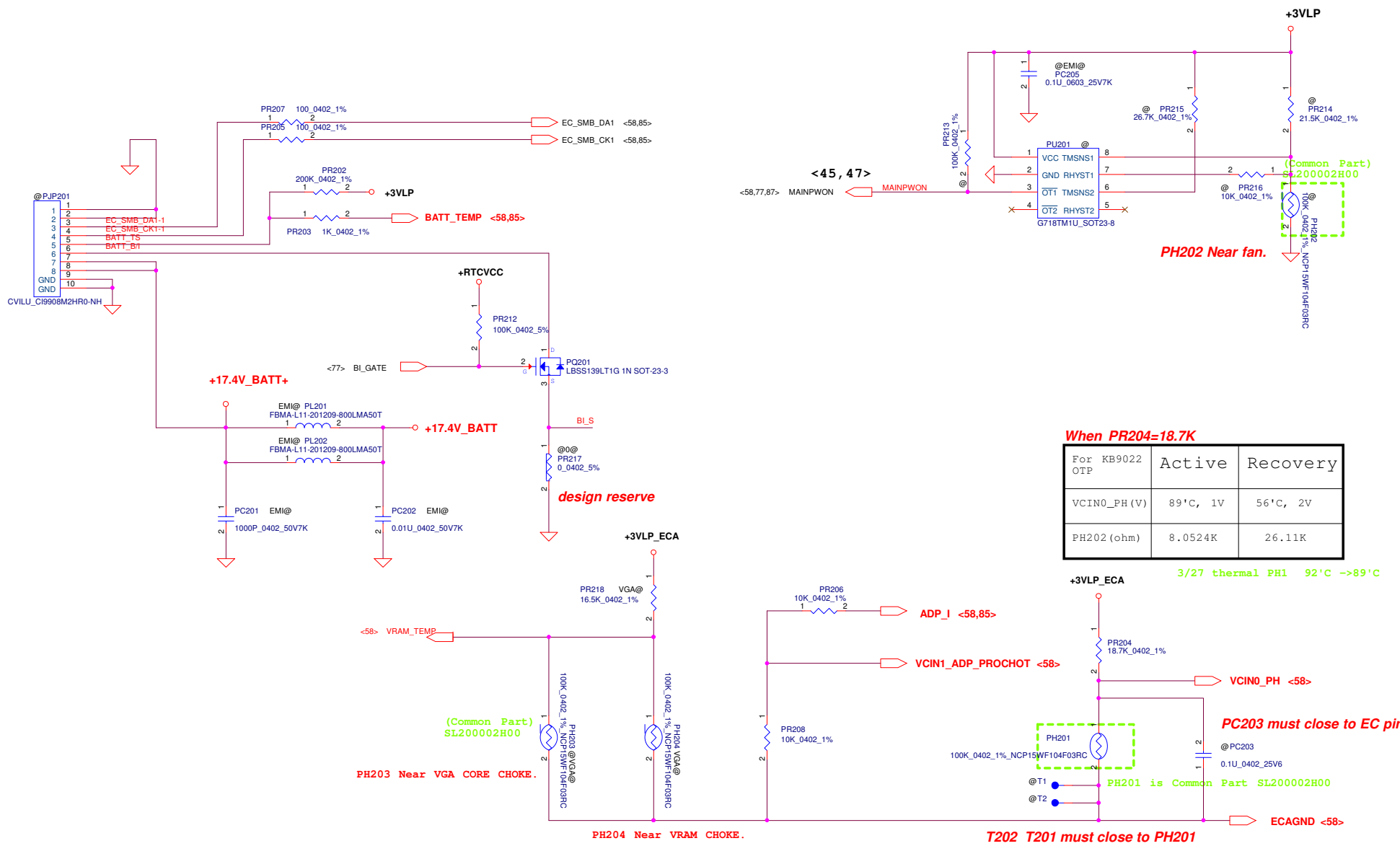
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Issued Date	2020/07/07	Deciphered Date	2020/09/20	Title DCIN		
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				Date:	Tuesday, December 01, 2020	Sheet 82 of 121

Reserve Page

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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 83 of 121

Battery Bot Side

- PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+



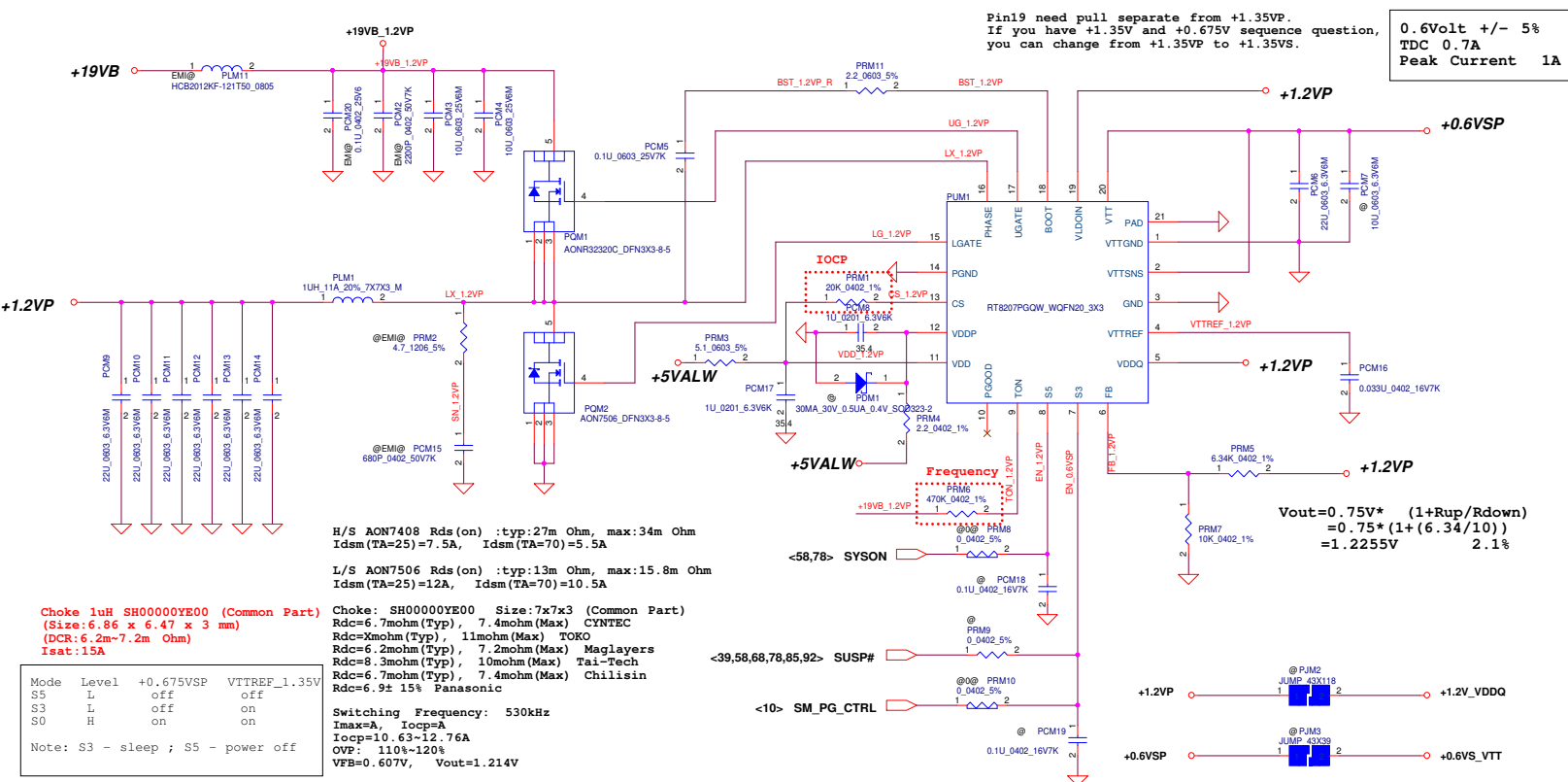
$$ADP_I = 20 * I(\text{adapter}) * 0.01$$
$$I(\text{adapter}) = \text{adapter (W)} * 130\% / 19$$

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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 86 of 121

Reserve Page

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				Size	Document Number	Rev
					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 88 of 121



Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A

Choke 1uH SH00000YE00 (Common Part)
(Size:6.86 x 6.47 x 3 mm)
(DCR:6.2m-7.2m Ohm)
Isat:15A

Mode Level +0.675VSP VITREF_1.35V
S5 L off off
S3 L off on
S0 H on on

Note: S3 - sleep ; S5 - power off

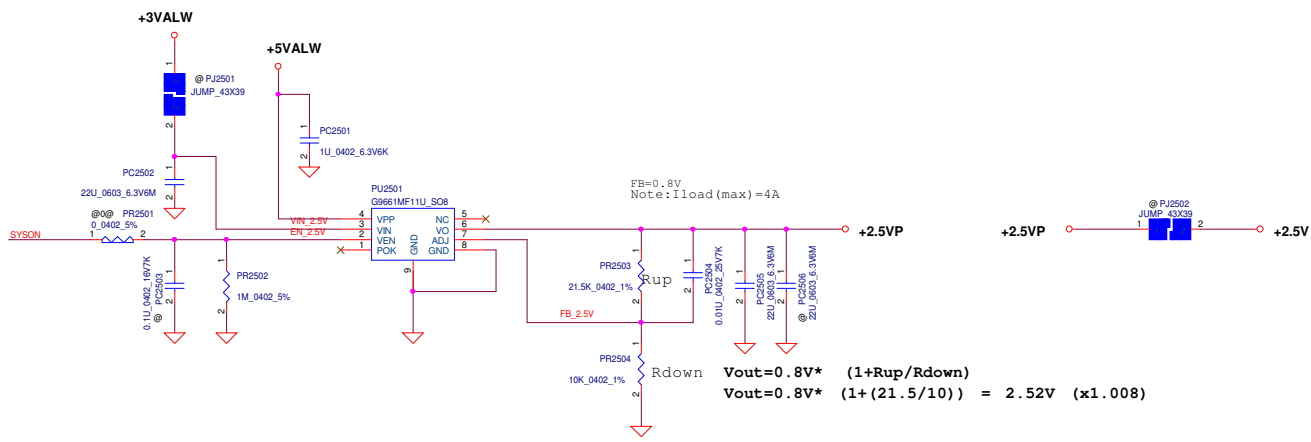
H/S AON7408 Rds(on) :typ:27m Ohm, max:34m Ohm
Idsm(TA=25)=7.5A, Idsm(TA=70)=5.5A

L/S AON7506 Rds(on) :typ:13m Ohm, max:15.8m Ohm
Idsm(TA=25)=12A, Idsm(TA=70)=10.5A

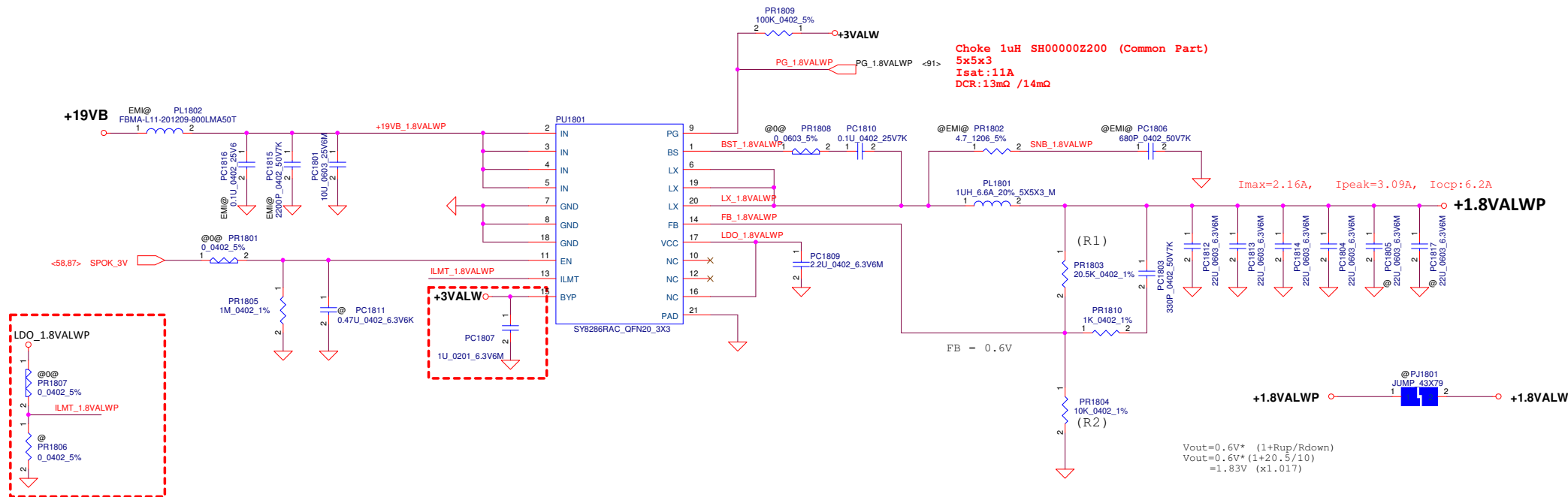
Choke: SH00000YE00 Size:7x7x3 (Common Part)
Rdc=6.7mohm(Typ), 7.4mohm(Max) CYNTEC
Rdc=Xmohm(Typ), 11mohm(Max) TOKO
Rdc=6.2mohm(Typ), 7.2mohm(Max) Maglayers
Rdc=8.3mohm(Typ), 10mohm(Max) Tai-Tech
Rdc=6.7mohm(Typ), 7.4mohm(Max) Chilislin
Rdc=6.9±15% Panasonic

Switching Frequency: 530kHz
Imax=A, IoCP=A
IoCP=10.63~12.76A
OVP: 110%~120%
VFB=0.607V, Vout=1.214V

$$V_{out} = 0.75V * (1 + R_{up}/R_{down})$$
$$= 0.75 * (1 + (6.34/10))$$
$$= 1.2255V \quad 2.1\%$$



$$V_{out} = 0.8V * (1 + R_{up}/R_{down})$$
$$V_{out} = 0.8V * (1 + (21.5/10)) = 2.52V \quad (x1.008)$$



8288RAC

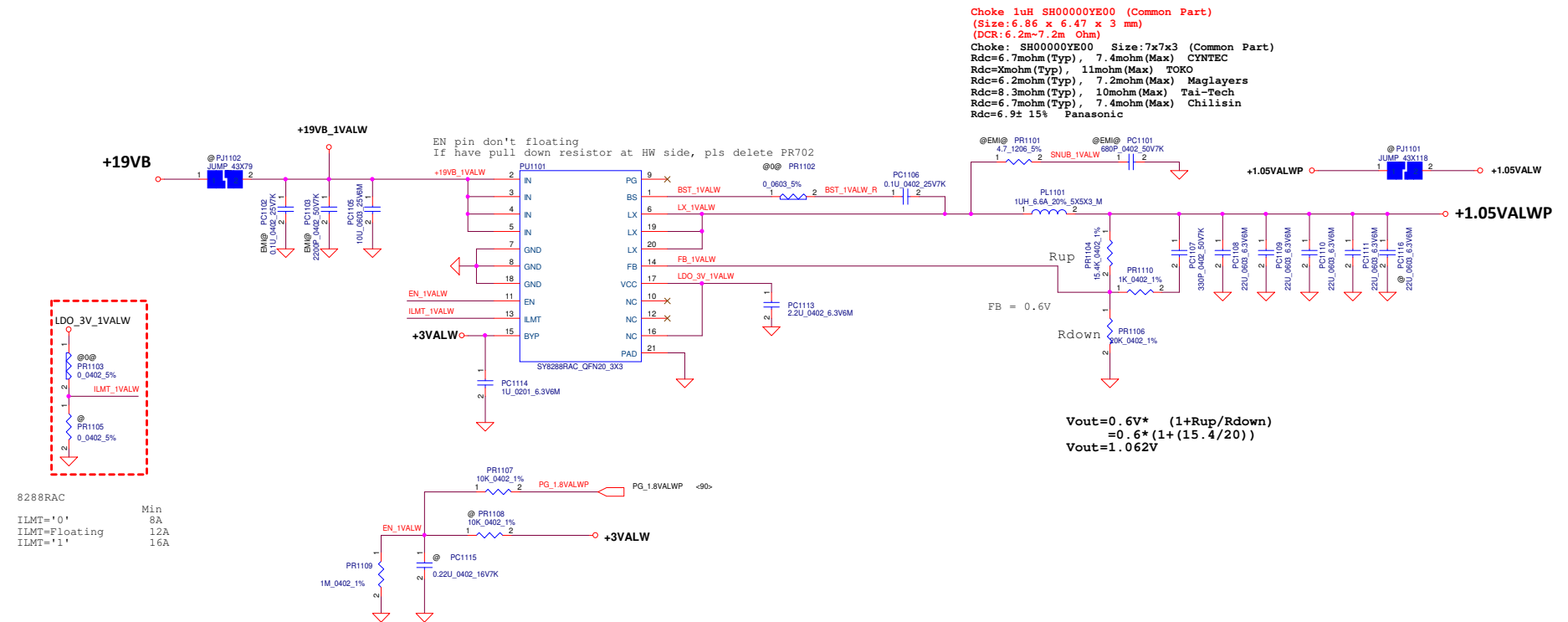
Min

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ILMT='Floating' 12A

ILMT='1' 16A

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				Size	Document Number	Rev
					GXXXX LA-XXXXP	0.1
Date: Tuesday, December 01, 2020				Sheet	90	of 121



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				Document Number	0.1
				Date	12/01/2020
				Sheet	91 of 121

Reserve Page

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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 93 of 121

Reserve Page

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					GXXXX LA-XXXXP	0.1
Date: Tuesday, December 01, 2020				Sheet	94 of 121	

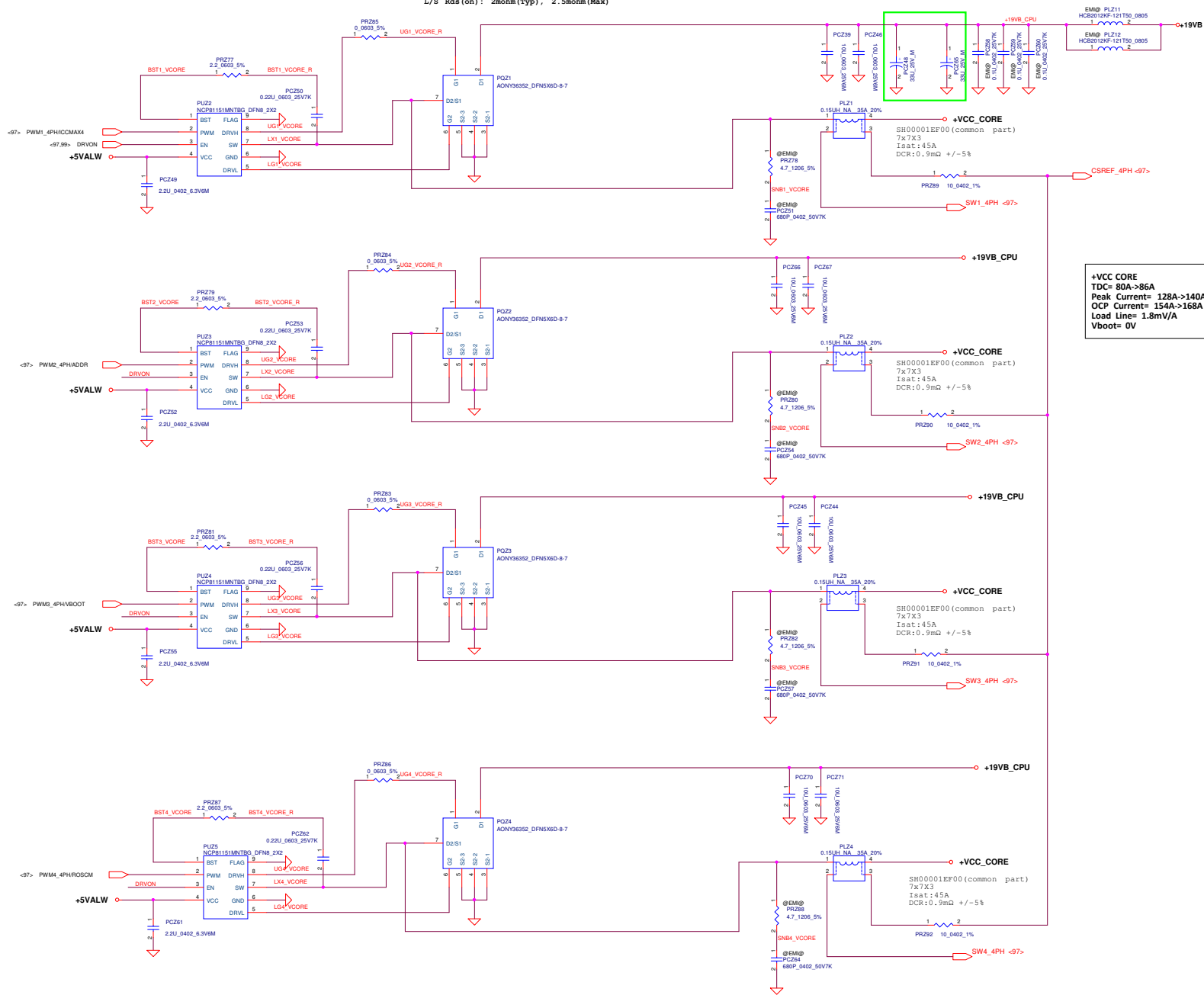
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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 95 of 121

Reserve Page

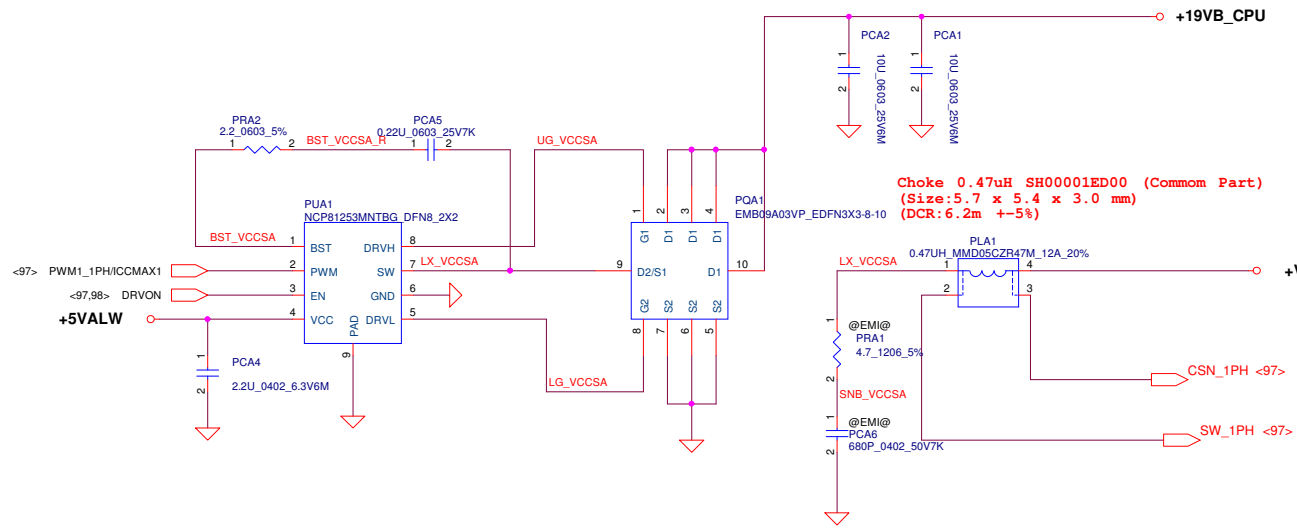
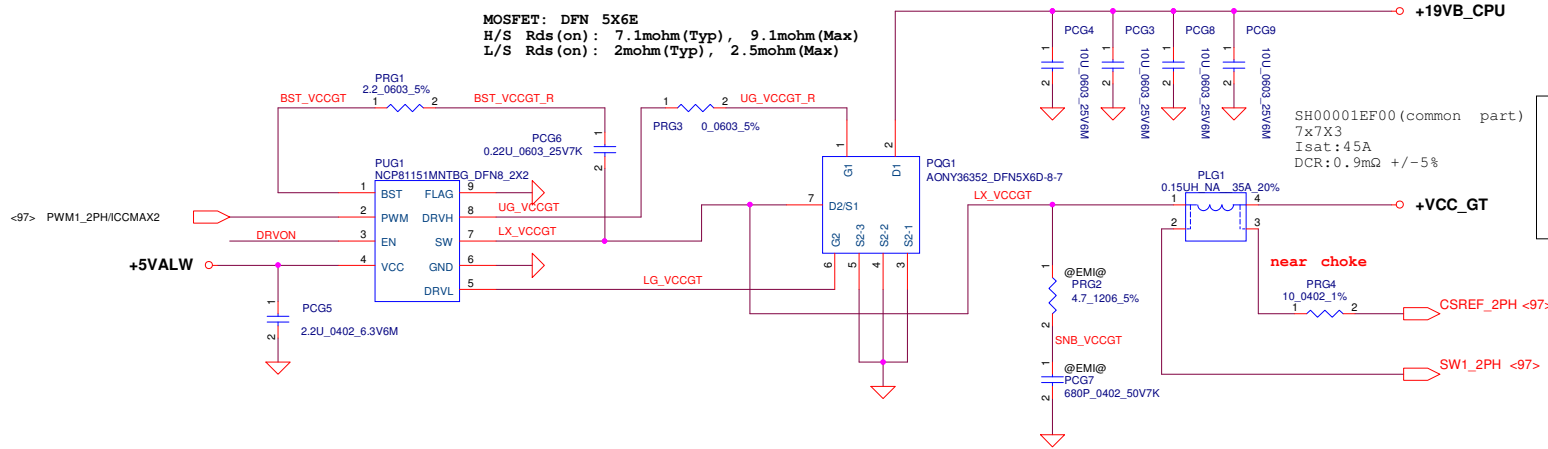
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				Date:	Tuesday, December 01, 2020	Sheet 96 of 121

MOSFET: DFN 5X6E
R/S Rds (on) : 7.1mohm(Typ) , 9.1mohm(Max)
L/S Rds (on) : 2mohm(Typ) , 2.5mohm(Max)



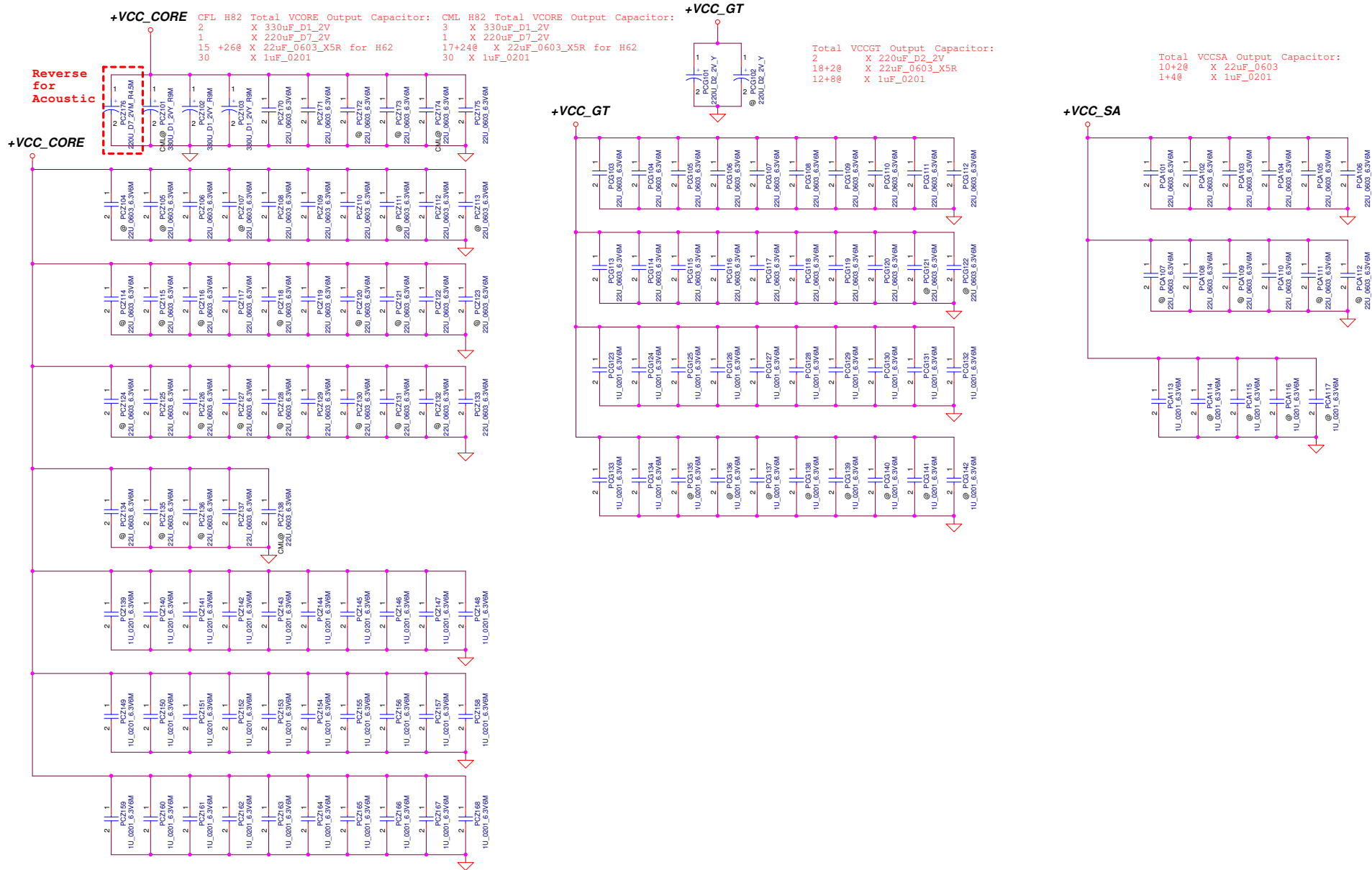
+VCC CORE
TDC= 80A->96A
Peak Current= 128A->140A
OCP Current= 154A->168A
Load Line= 1.8mV/A
Vboot= 0V

Main Func = VCCGT/+VCCSA



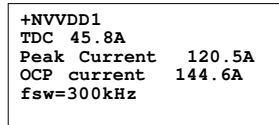
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				Date:	Tuesday, December 01, 2020	Sheet	100 of 121

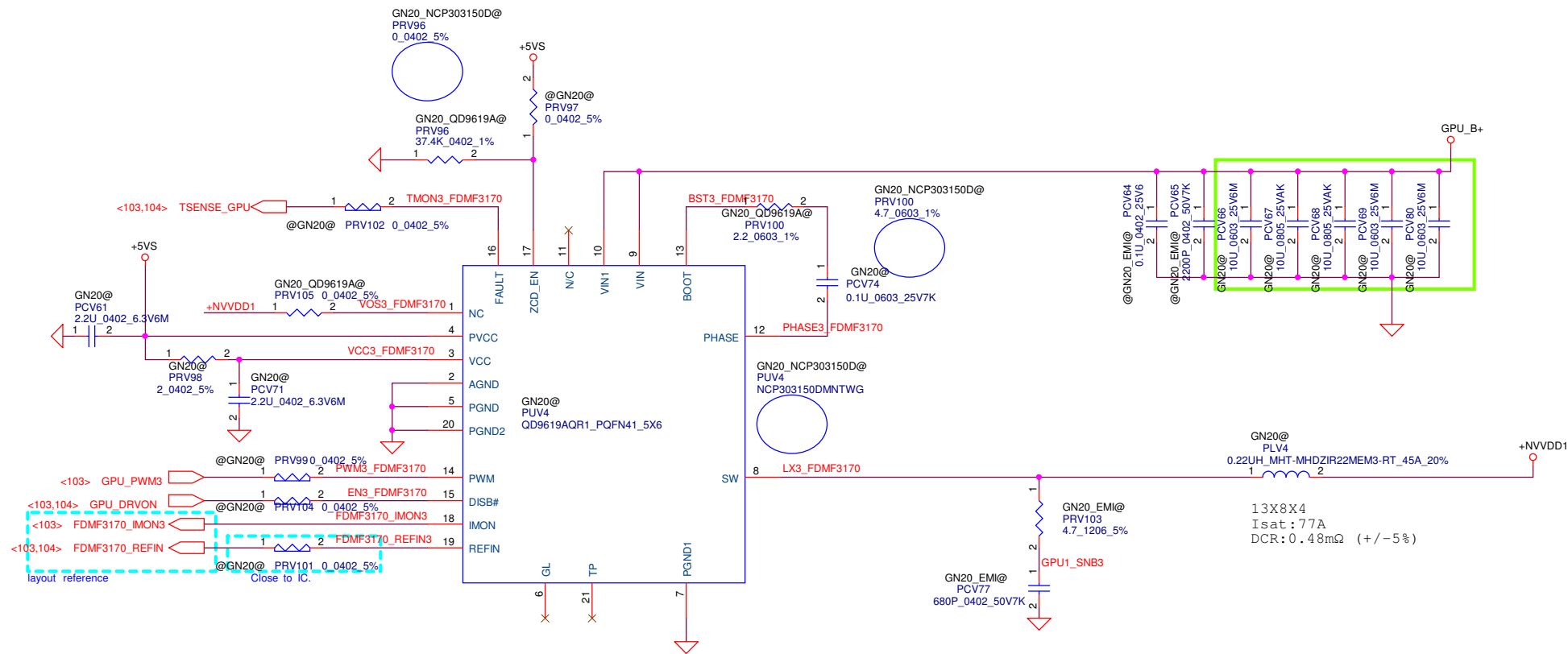


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					GXXXX LA-XXXXP	0.1
Date: Tuesday, December 01, 2020				Sheet	102 of 121	



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				Document Number	0.1
				GXXXX LA-XXXXP	
Date:				Tuesday, December 01, 2020	Sheet 104 of 121

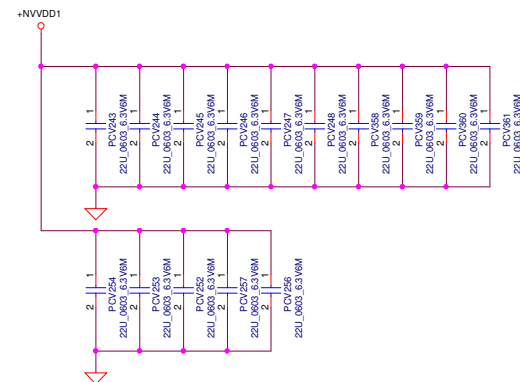
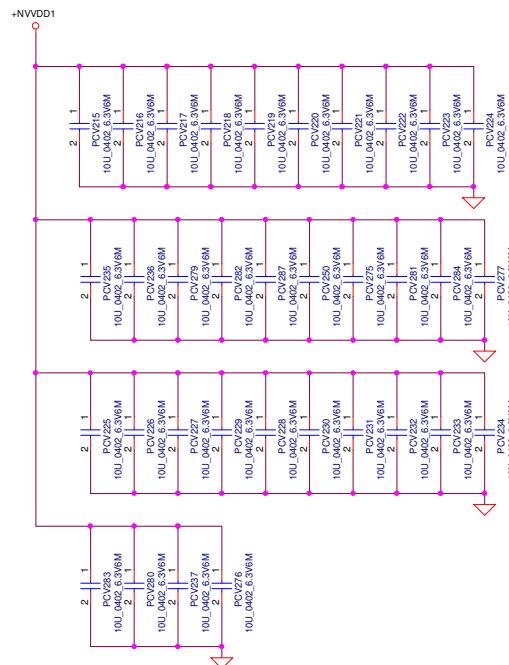
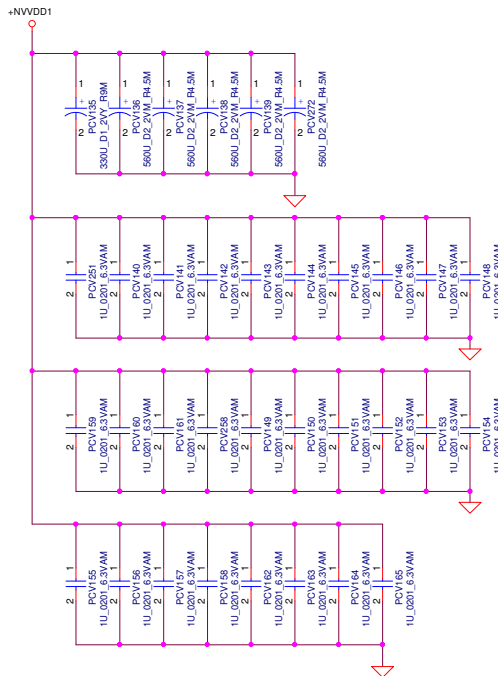


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					Reserve
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					GXXXX LA-XXXXP
					Rev 0.1
					Date: Tuesday, December 01, 2020
					Sheet 105 of 121

Reserve Page

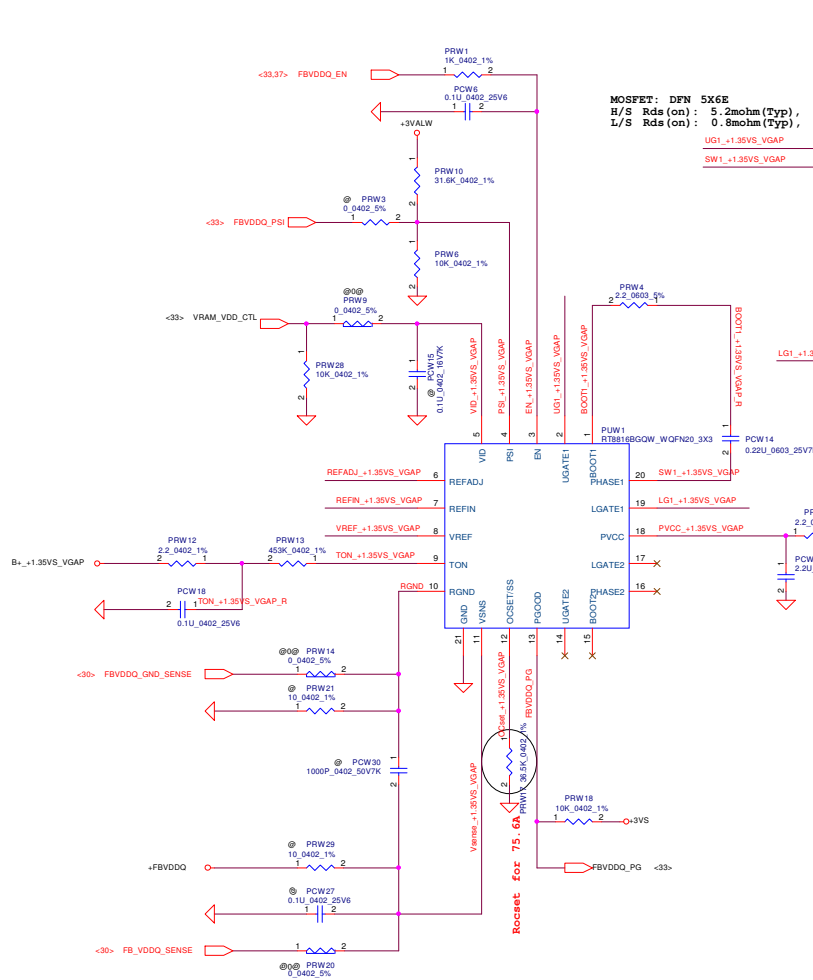
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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 106 of 121

+NVVDD
560uF X 6
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28



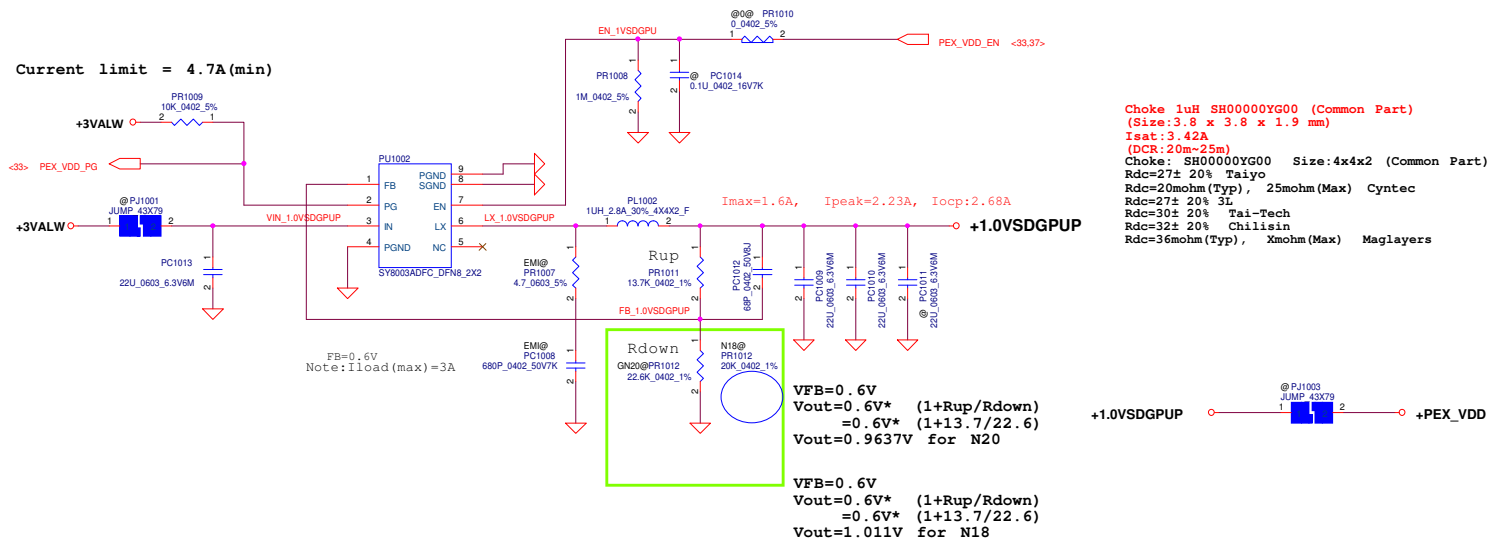
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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 109 of 121



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Issued Date	2020/07/07	Deciphered Date	2020/09/20	Title	1.05VSDGPU
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				Date	102009, December 01, 2020
				Sheet	110 of 121
				Rev	0.1

Reserve Page

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				Document Number		
				Rev		
				Date: Tuesday, December 01, 2020		
				Sheet 111 of 121		

Reserve Page

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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 112 of 121

Reserve Page

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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 113 of 121

Reserve Page

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					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 114 of 121

Reserve Page

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Issued Date	2020/07/07	Deciphered Date	2020/09/20	Title Reserve		
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Date: Tuesday, December 01, 2020				Sheet	115 of 121	

Reserve Page

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				Size	Document Number	Rev
					GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 116 of 121

Reserve Page

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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					GXXXX LA-XXXXP	0.1
Date: Tuesday, December 01, 2020				Sheet	117	of 121

Reserve Page

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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Date: Tuesday, December 01, 2020				Sheet	118 of 121	

Page 1 of 1 for
PWR

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Issued Date	2020/07/07	Deciphered Date	2020/09/20	Title	PIR	
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				Custom	GXXXX LA-XXXXP	0.1
				Date:	Tuesday, December 01, 2020	Sheet 119 of 121

Version change list
(P.I.R. List)

Page 1 of 1 for
PWR

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92	change PR1009 from 100K_0402_5%(SD028100380) to 10K_0402_5%(SD028100280) change PG pull high from +3VS to +3VALW change PRW1 from 20K_0402_1%(SD034200280) to 1K_0402_1%(SD034100180) Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSD6PU to Vsense_+1.35VS_VGAP. unpop PCV135 Change the PUV8, PCV9 from pop to un-pop. Add location PRV51 0_0402_5%(SD028000080), and pop. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Delete PL1111 (HCB2012KF-121T50_0805)	11/14	A
02	Design Update	solution change	83, 85 90, 91	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00) update location PR65 PRA3 to PUG1 PUA1 PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00) pop PQZ2, PQZ4 unpop PQZ1, PQZ3	11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91	Change PRM10, PRM8, PRV82, PRV85, PRV92, PRV95, PRV79, PRV81, PRV84, PRV89, PRV91, PRV94, PRV54, PRV56, PRV70, PRV145, PRV146, PRZ72, PRZ73, PRZ25, PRZ30, PRZ32, PRZ18, PRZ9, PRZ11, PRZ24, PRZ27,PRV20, PRV34	11/16	A
04	Design Update	For CPU transient	89, 92	change PRZ12 from 1.78K_0402_1%(SD00000WY80) to 1.62K_0402_1%(SD000003380) change PRZ14 from 31.6K_0402_1%(SD034316280) to 28K_0402_1%(SD034280280) change PCZ24 from 470P_0402_50V8J(SE071471J80) to 220P_0402_50V8J(SE082221J80) change PRZ51 from 84.5K_0603_1%(SD014845280) to 100K_0603_1%(SD014100380) PRZ61=110k ohm @H82, PRZ61=102k ohm @H62 PRZ35=25.5k ohm @H82, PRZ35=28k ohm @H62 unpop PCZ101, PCZ103, PCG102 pop PCZ176 un pop PCZ120, PCZ104, PCZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124 for H82 un pop PCZ120, PCZ104, CZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124, PCZ123, PCZ127, PCZ107, PCZ113, PCZ116, PCZ114 for H62	11/19	A
05	Design Update	solution change	84	Change the PL501 1.5uH to common part Change the PCZ47, PCZ48, PCZ65, PCV36, PCV249 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_M (SF000007700) Chnage the PRZ43 from 12.1K_0402_1%(SD034121280) to 12K_0402_1%(SD034120280)	12/3	A
06	Design Update	solution change	87	unpop PC1811 0.47U_0402_6.3V6K (SE124474K80)	12/12	B
07	Design Update	solution change	83, 97	pop PCV149~PCV158, PCV162~PCV165, PCV258 (1U_0201_6.3V6M) reserve PDB2 for dead battery	12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B
09	Design Update	For ESD request	82	Pop PC205 0.1U_0603_25V7K (SE042104K80) HS 鋁皮電鍍 ESD 能量吸收板 及 HS cable coupling 銅板造成 ESD	1/15	B
10	Design Update	For EMI request	93, 96	Pop PCW1, PCV48 2200P_0402_50V7K (SE074222K80) for EMI request Pop PCW2, PCV47 0.1U_0402_25V6 (SE000006880) for EMI request	1/15	B
11	Design Update	Design change	90, 87	delete boost circuit and PCZ47	5/7	FH58F EVT
12	Design Update	Design change	90, 87	delete PC1112	5/7	FH58F EVT
13	Design Update	Design change	88, 93	change PCB15 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to 1U 16V K X5R 0402(SE000000U00) change PCB16 from S CER CAP 1U 6.3V K X5R 0402(SE000000K80) to S CER CAP 2.2U 16V K X5R 0402(SE000013780) Add PLV2, PLV3 second source S COIL .22UH TMP1004H-R22MG-R5505-D 50A(SH00001XH00)	6/25	INV2
14	Design Update	change CH_OC to 75A	95	change PRV71 from S RES 1/16W 133K +-1% 0402(SD034133380) to S RES 1/16W 113K +-1% 0402(SD034113380)	6/25	FH58F PVT

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				PIR	
				Document Number	
				GXXXX LA-XXXXP	
				Rev	
				0.1	
				Date: Tuesday, December 01, 2020	
				Sheet 120 of 121	

Phase Rev.

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PIR-HW1

Document Number
GXXXX LA-XXXXF

Tuesday, December 01, 2020	Sheet	121	of	121
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